BEATING THE ATE SLUMP BY CUTTING COSTS / 76

COMPUTER-AIDED TESTING GETS REAL / 81

A PENTON PUBLICATION IN U.S. $6.00 NOVEMBER 1989

Electronics®

MAKING THE RIGHT MOVES IN THE ASICs GAME

PAGE 56

NOW THERE'S CAD FOR ANALOG AND MIXED-SIGNAL ICs...

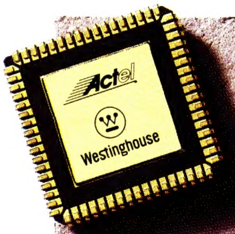
PAGE 62

...AS BiCMOS MAGIC EASES THE JOB FOR VENDORS

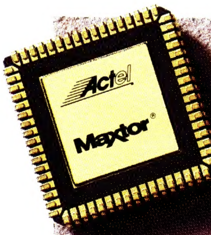
PAGE 67

28 NOV 1989

Logic In For The



Westinghouse military systems engineers replaced four 22V10 PALs and six MSI devices with a single ACT 1010 part, handling the entire error correction, registration, and interface logic for their high speed, high dynamic range A/D converters. Schematics were captured on a Mentor system, and implemented with the Action Logic System (ALS). The design utilized 224 out of 295 logic modules.



Maxtor engineers use Actel's ACT 1010 chips and the Action Logic System software to quickly create and modify new disk drive electronics. They've produced nine different designs, with 85% to 95% gate utilization. During seven months of intensive work the ALS software has never crashed or lost data, and the system has produced every part as designed.

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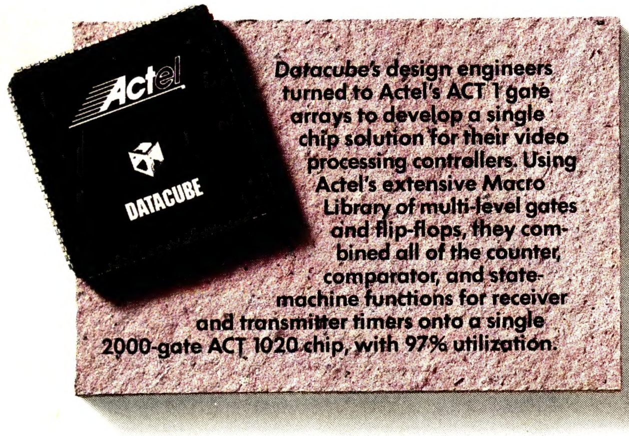
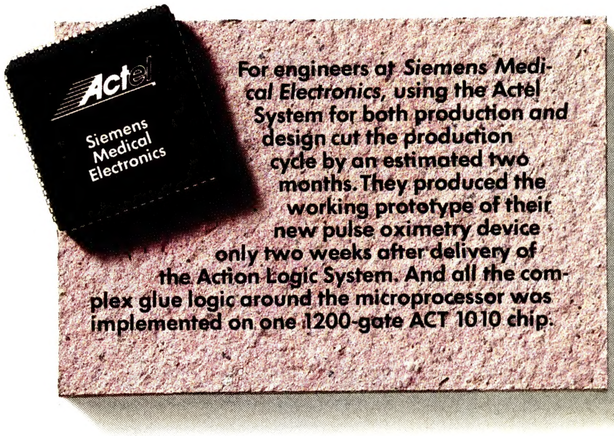


Datacube's design engineers turned to Actel's ACT 1 gate arrays to develop a single chip solution for their video processing controllers. Using Actel's extensive Macro Library of multi-level gates and flip-flops, they combined all of the counter, comparator, and state-machine functions for receiver and transmitter timers onto a single 2000-gate ACT 1020 chip, with 97% utilization.



For engineers at *Siemens Medical Electronics*, using the Actel System for both production and design cut the production cycle by an estimated two months. They produced the working prototype of their new pulse oximetry device only two weeks after delivery of the Action Logic System. And all the complex glue logic around the microprocessor was implemented on one 1200-gate ACT 1010 chip.

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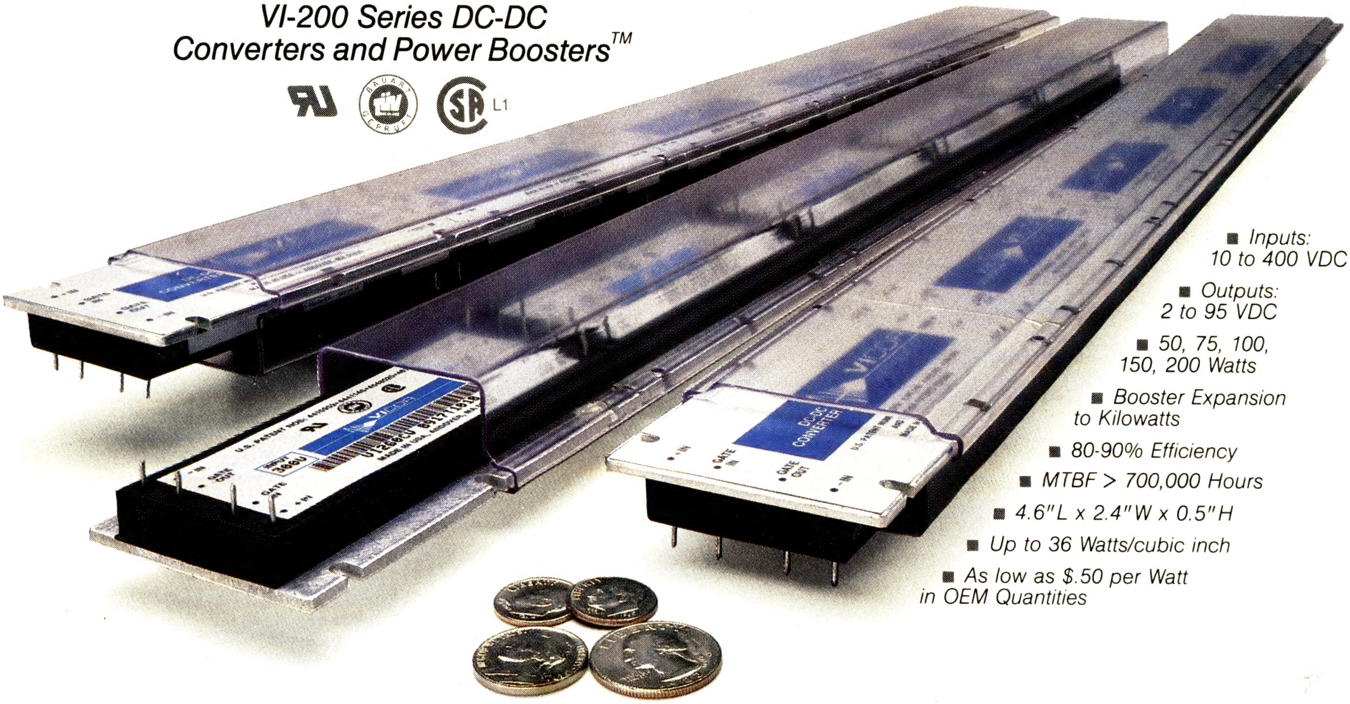

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EARTHQUAKE!

For Silicon Valley, life goes on after the big shake—and life these days in the chip business is spelled "ASIC"

All of us in the world outside northern California who watched day after day the starkly graphic TV pictures of the Oct. 17 earthquake could be forgiven for thinking of the event as the "San Francisco Bay earthquake." After all, that's what we saw on TV—the frightening Marina district fire in San Francisco on the Tuesday night of the earthquake, the horribly collapsed Nimitz Freeway in Oakland the next day when the sun came up.

Almost forgotten, perhaps because a seriously wounded San Francisco itself was so deeply involved, was the fact that the epicenter of the earthquake was near Santa Cruz, and that the rumbling and shaking and rolling phenomenon had its way with a 60-mile-long stretch of northern California that forms what is known as Silicon Valley. Amid the personal human tragedies, there was the potential also for a crippling industrial tragedy, one that would have meant deep and serious trouble for what has become one of the nation's basic industries: electronics.

But the electronics community was lucky. That is particularly true of the semiconductor industry, which is so firmly rooted in—and dependent upon—the valley of its birth. The quake, a 7.0 monster that was less severe than the fabled one in 1906, caused relatively minor damage to equipment, as executive editor Jonah McLeod makes clear in his story on p. 31, although the people who work in the plants and offices were variously affected as homes and highways sustained damage ranging from hairline cracks to gaping fissures. The fab lines and assembly operations of Silicon Valley survived.

This time. The sobering thought for electronics executives as the people of the region put their lives back together and consider what to do the next time—we are told that the Oct. 17 temblor was not the long-promised and anticipated "big one"—focuses on "What do we do now?" How does an industry make itself earthquake-proof when the scientists and engineers tell us there's no such thing? And in strictly human terms, those that transcend science and engineering, how do the people who work in the industry ever manage to get back to ordinary living without looking over their shoulders every time they hear a loud noise? The prospect of having to go through the same thing or worse is truly frightening.

Until the people who run the companies that make up the semiconductor industry figure out the answers to those questions—if indeed there are answers—life among the chips goes on, as it must.

The buzzword these days is "ASICs," and these days ASICs are coming of age. The cover article on p. 56 by Bernard Cole bears witness to that simple truth.

The most striking feature of the maturing of the ASIC revolution is the increasingly global nature of the business. As the cover story makes amply clear, the ASIC chess game has gone beyond a contest between Japan and the U. S. It has become a veritable tournament, with manufacturers in Asia and Europe making runs at the segments now dominated by the two big boys. The prize is indeed worth jousting for: $12.5 billion and 21% of all IC sales by 1993.

It's a good lesson for these sometimes frightening times: come earthquake or high water, the unquenchable innovative and competitive spirit that distinguishes the chip business continues to drive it. And that's the way it should be.

HOWARD WOLFF

November 1989 Volume 62, Number 11

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NOVEMBER 1989

Electronics

NEWSLETTERS

Electronics, 19
- Japan closes in on a parallel inference machine . . .
- . . . as U. S. companies learn how to sell technology in Japan
- IBM gets ready to unleash its next-generation RISC processor . . .
- . . . while DEC's VAX 9000 takes dead aim at IBM mainframes
- HP's Team Computing makes multivendor networking easier
- Intel-Alliant standard spurs 860 in parallel computing

Products to Watch, 23
- Silicon Graphics opens its graphics library to third-party vendors
- Hewlett-Packard integrates low-cost X-Window terminals into its work station line
- Intel pushes its real-time operating system to 32 bits
- Harris's 80C286 beats the competition to the punch on MIL-STD-883
- Space-saving burn-in unit heats with high-frequency conductive technique

European Observer, 53
- Will the telecom merger mania continue to spread?
- West Germans put more cash into Jessi
- Sliding DRAM prices should mean cheaper SRAMs
- MIPS, Nixdorf to blend muscle in RISC technology

FEATURES

COVER: Making the right moves in ASICs, 56
As the playing field shifts, vendors are retooling products, rethinking strategies, and readying themselves for intensified global competition

- **Analog gets automated, 62**
Silicon Compiler Systems offers the first circuit and layout synthesis tools for analog and mixed-signal devices
- **Mixed-mode magic, 67**
LSI Logic's LAD310 series is the most ambitious attempt to date to satisfy the demand for more powerful mixed-signal ASICs

How the U. S. is fighting back in trade, 70
Thanks to the Omnibus Trade Act of 1988, the U. S. International Trade Commission is finally becoming a potent force for high-tech outfits conducting international business

Bringing down the costs of ATE, 76
Vendors of automatic test equipment are playing all the angles in an effort to give customers what they want: powerful systems at affordable prices

- **Computer-aided testing gets real, 81**
The S790 from Schlumberger gives test engineers the same kind of power and flexibility that design engineers enjoy on work stations
- **Scalable system concept hits ATE, 85**
Teradyne's new linear-IC tester, the A510AL, provides three levels of user configurability

Voice processing reaches out to touch everyone, 88
The industry is on the brink of adopting a voice-processing specification that will let multivendor systems communicate

Make room for pocket computers, 93
Battery-powered models are the fastest-growing segment in the business—and the 1-lb machines are the talk of the show at Comdex

Looking ahead to FDVDI, 99
A proposed follow-on to FDDI can fully integrate voice, data, and video transmission—and a chip set is on the way

This printer takes on Presentation Manager graphics, 103
QMS unveils the first system to directly support the PM imaging model

VOLUME 62, NO. 11

WORLDWIDE NEWS ANALYSIS

Probing the News

Military, 29
Defense firms face the music: it's not going to get better

The Earthquake, 31
All in all, for Silicon Valley it could have been worse

OLTP, 32
Tandem's new Cyclone system blows away the competition

Shows, 38
Broader in scope, a revamped Wescon makes its stand

RISC Boards, 40
Board makers ride the RISC bandwagon—and most choose Intel's i860 and i960 processors

Microcontrollers, 43
Siemens gets ready with a homemade 16-bit bombshell

Portables, 44
Here's the first notebook-size PC with a hard-disk drive

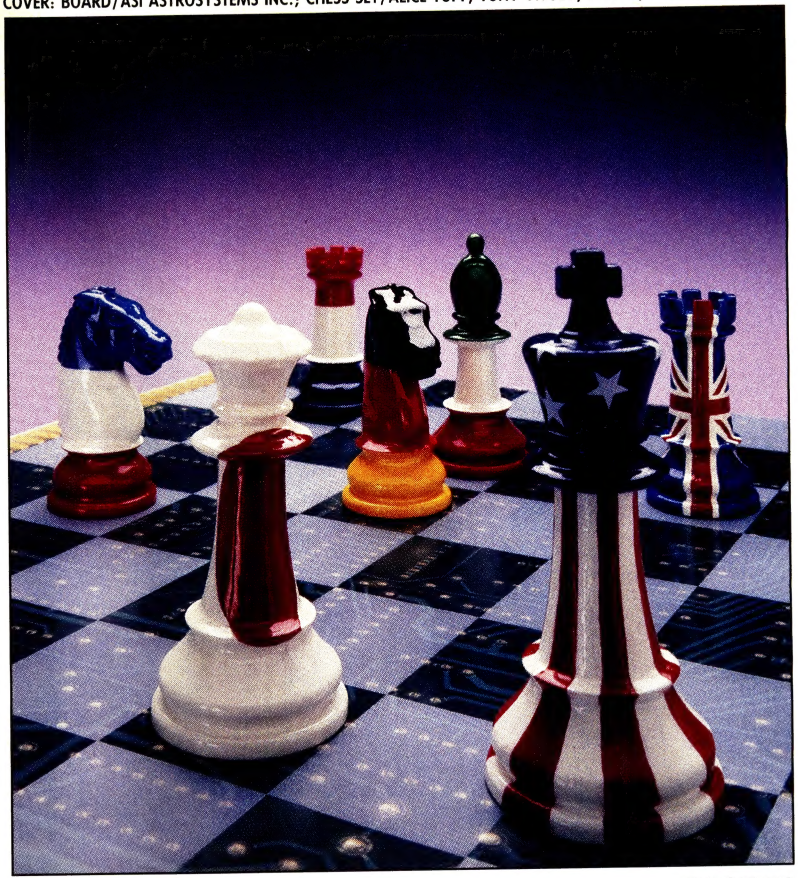
Consumer, 52B
From ITT Semiconductors, an IC to decode all TV sound signals

Lasers, 52D
A startup is the surprise winner in slab laser race

Personal Computers, 52F
U. S.-based Tandy buys into Europe's PC market

ISDN, 52F
Nynex finds a unique development partner: the British crown colony of Gibraltar

COVER: BOARD/ASI ASTROSYSTEMS INC.; CHESS SET/ALICE TOPF, TONY VITOLO; PHOTO/WILLIAM COSTELLO



PAGE 56

COMPANIES TO WATCH

Cirrus Logic Inc., 107
Flush with cash after going public, the chip maker hits the acquisition trail

Synopsys Inc., 108
This design-automation outfit has the right tools at the right time

Western Digital Corp., 110
The company is becoming the one-stop shopping source for PC vendors—and racking up $1 billion in sales this year

PEOPLE TO WATCH

Marie Monique-Steckel, 112
The president of France Telecom embarks on a search for strategic partners in the U. S.; she's treating Europe '92 as a once-in-a-century marketing opportunity

DEPARTMENTS

Up Front, 3
For northern California chip makers, life goes on after the big shake—and these days life is spelled "ASIC"

Readers Report, 8

Letter from Orange County, 12
California's "Big Orange," once a no-man's land for high-technology companies, is becoming the state's biggest growth spot

Update, 120
Vendors charge ahead with speedier RISC chips; one new device from Bipolar Integrated Technology runs at 65 mips, and some companies are shooting even higher, to 100 mips or more

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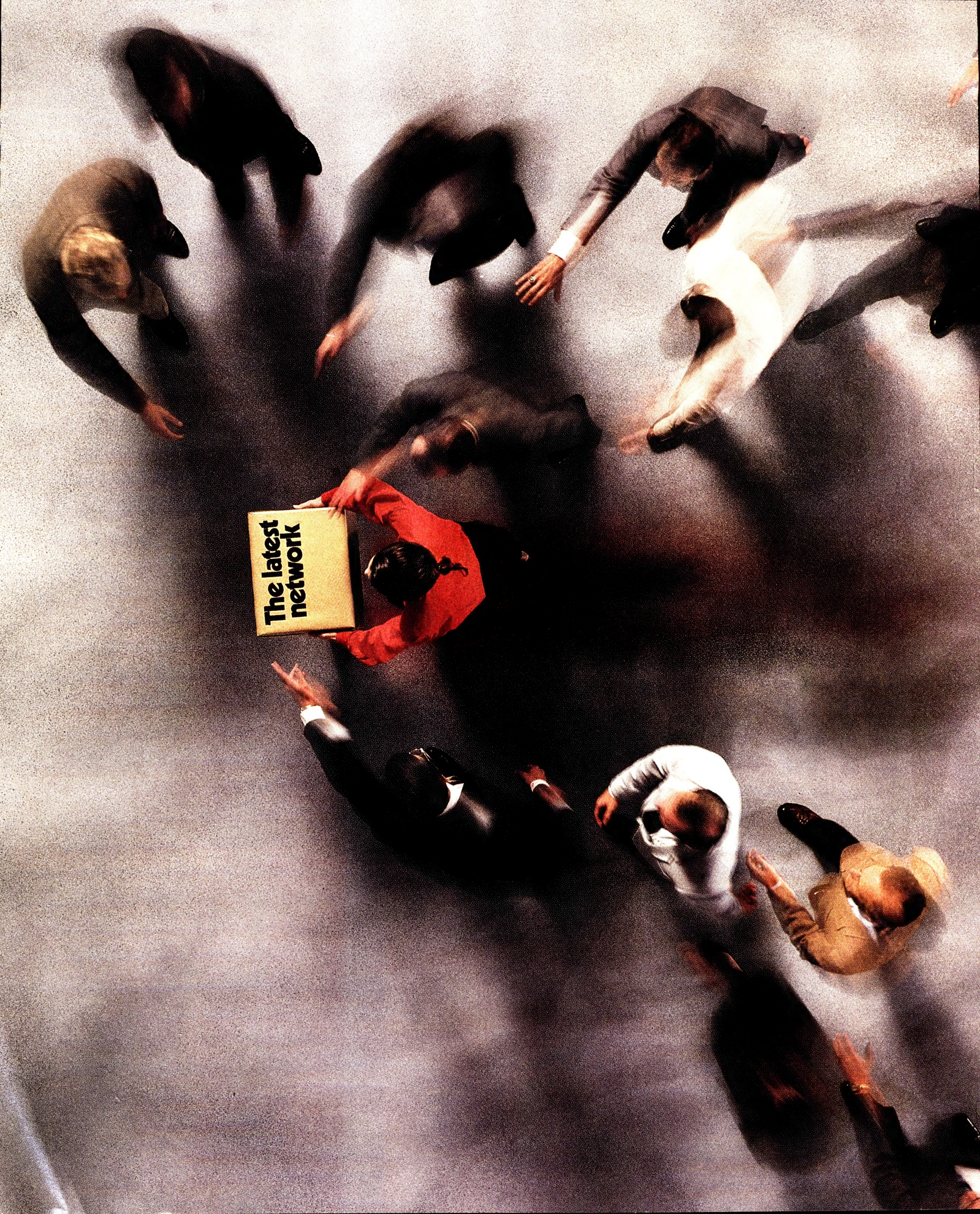

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*According to a Dataquest Report, October 1988 for the year 1987. Stated in dollars.

Circle 215

Make technology the victor

To the editor: Your position in "Technology vs. terror" [*Electronics*, July 1989, p. 46] concerning airport security was just great. But I wonder why you were willing to limit the application of TNA (thermal neutron activation) devices just to the baggage. My 39 years of experience with neutron-activation analyses tells me that we can never fly safely on international flights until every *person* on board and everything that they carry have been scanned.

Those of us who have worked with ultraviolet light detectors and neutron activation know that all that must be done to have technology vs. terror come out in favor of technology is to get rid of the silly regulations that have caused the economic demise of the nuclear option.

Galen Winsor
Kennewick, Wash.

Feeling left out . . .

To the editor: "Hard times in rad-hard" [*Electronics*, May 1989, p. 82] was an excellent overview. However, it contained a glaring omission: the work ongoing at the Westinghouse Advanced Technology Laboratory in Baltimore.

Westinghouse has developed and demonstrated the densest silicon-on-insulator design rules, including 1.0-µm gates with unrestricted 3.0-µm first-metal pitch and 4.0-µm second-metal pitch. We have fabricated several VLSI device types on 4-in. (not limited to 3-in., as stated in the article) silicon-on-sapphire wafers, and demonstrated "best-wafer" yields comparable with bulk silicon on a 16-Kbit static random-access memory that is part of a test-pattern drop-in on product wafers.

Westinghouse believes there are potential benefits to migrating from SOS wafers to other forms of SOI starting wafers, such as Simox and ZMR, as they become more mature. We have demonstrated the transportability of the 1.0-µm CMOS SOS process to other forms of SOI starting wafers by producing the first 16-Kbit SRAM on both Simox and ZMR starting wafers.

M. L. Richardson
Marketing Manager
Westinghouse Corp.
Advanced Technology Division
Baltimore

. . . and disturbed

To the editor: I am disturbed by "Hard times in rad-hard." First, you left out my company, Vitesse Semiconductor, as a key company in gallium arsenide. Second, I am disturbed by the fact that the U. S. military, Darpa, the Star Wars organization, etc. are ignoring the opportunity to achieve a very high rad-hard rating with very high density, very competitively priced GaAs LSI devices.

GaAs merchant vendors such as Gigabit, Triquint, and Vitesse have made considerable progress in the last few years. Processes are stable, yields are good. In fact, GaAs is probably less expensive than SOS or SOI.

Vitesse is delivering GaAs gate arrays ranging in complexity from 2,000 to 16,000 gates. Standard TTL and/or emitter-coupled-logic power supplies and input/output levels are the norm. Speed is in the range of 250 MHz to 2.5 GHz, and power supply is 25% to 50% that of TTL or ECL at the same speed. Prices are the same as silicon arrays of the same complexity. Our data confirms the superior performance of GaAs in rad-hard environments, though I will concede that technologies such as SOS or SOI may be more suited than GaAs for high-density—64-Kbit and above—RAMs.

Pierre R. Lamond
Sequoia Capital
Menlo Park, Calif.

More than equipment

To the editor: While the equipment described in "Getting to the market on time" [*Electronics*, April 1989, p. 62] offers promise as far as more efficient wafer and chip modification, defect detection, CAD layout, and wafer processing are concerned, it takes more than equipment. It takes the right people with the right attitude and training.

For example, Orbit Semiconductor Inc. is the only semiconductor foundry that has no standard products of its own, the only one that provides custom process development, and the only one that gives customers a money-back guarantee that their delivery schedules will be met once the job is accepted. These are the intangibles.

Gary P. Kennedy
President
Orbit Semiconductor Inc.
Sunnyvale, Calif.

Amplification & Correction

In "Technology: the Wild Card" in the September issue, the die photos on p. 61 were from Toshiba America.

In the graph on p. 77 of the May issue showing the estimated number of reduced-instruction-set-computer chips shipped in 1988, the data shown was based on preliminary figures from Dataquest Inc. Here are the final numbers: AMD's AM29000, 1,000; Fujitsu's MB86900/S25, 12,500; Inmos's T414/800, 125,000; Intergraph APD's C100/C300, 13,700; Motorola's 88100, 6,000; Performance Semiconductor's R2/3000, 14,000; VLSI Technology's VL86C010, 3,500; others, 10,000.

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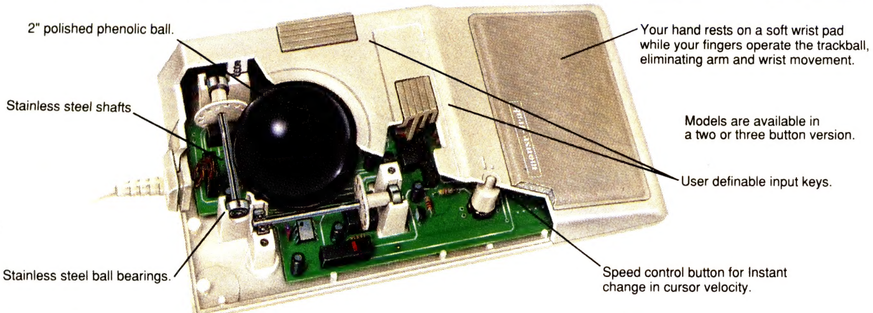
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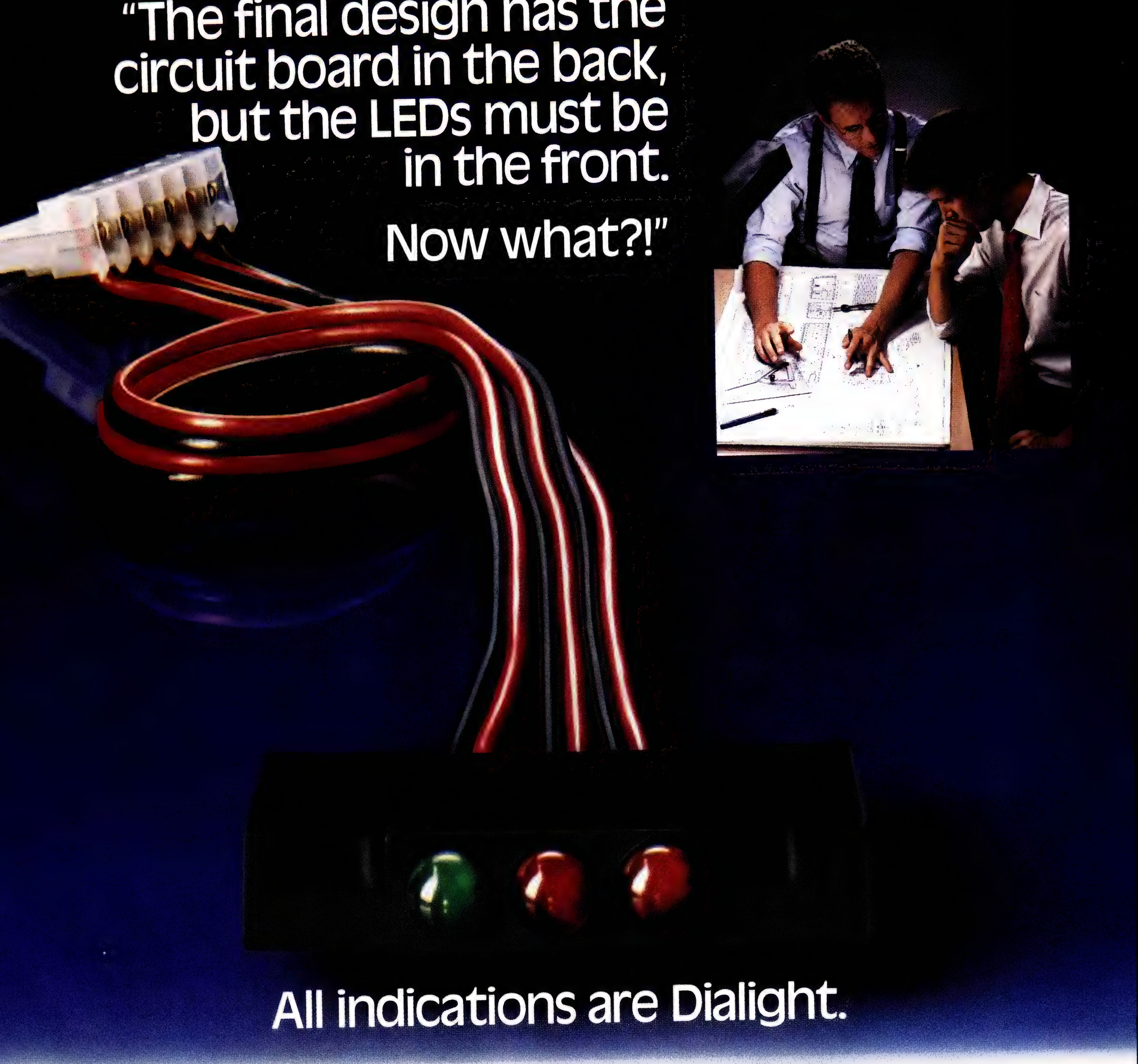
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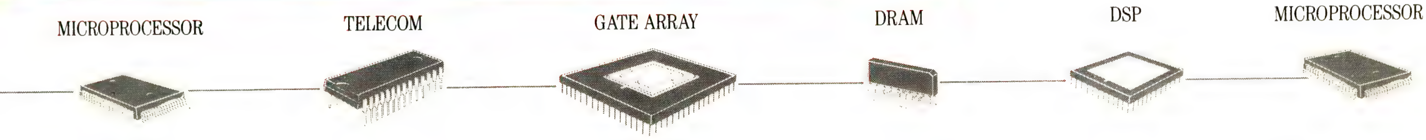

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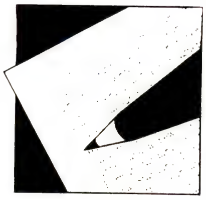
IN 'THE BIG ORANGE,' THEY'E SMILING AS THEY

IRVINE, CALIF.



Guess what has happened to Orange County? It has developed a high-tech soul.

For those not attuned to Southern California geography, Orange County is the stretch between Los Angeles and San Diego whose name once conjured up the image of a rural backwater dotted with orange groves and marked by rock-ribbed conservative politics. In high technology, it had a reputation as a place that never quite made it to the top. From the 1960s until about five years ago, many startups—especially in computers and peripherals—blasted off with high promise, never to be seen again.

That they faded in relative silence was another hallmark of the county, perhaps best summed up by the wisecrack that Orange County was a bunch of companies and suburbs whose only connection was the freeway.

That view also described the chief difference between the county and other places that became well-defined high-tech centers, with Silicon Valley as the prototype. Historically, the Big Gap hindering development efforts in the Big Orange was its lack of a central institution that could serve as a unifying force—and give focus to an area's people and activity—such as Silicon Valley's Stanford University.

But oh, how things have changed. Starting in 1985, a network of high-tech executives who make things happen began to emerge, as did a sense of excitement motivating workers. Why? "Several key developments support what's going on, but the University of California at Irvine is at the center of it," says Roger W. Johnson, chief executive officer of Western Digital Corp., the county's largest electronics company (see p. 110). UCI's contribution is superimposed on stunning growth over the past half decade in Orange County's industrial base, says the Irvine-based Johnson. That growth has been spearheaded by high-technology companies.

There is little specific data, since no government agency or industry research firm currently generates the information. But overall county figures for population and income show increases far exceeding those of the rest of California's major centers. Population has nearly doubled to more than 2 million in recent years, family median income passed $44,000 in 1988 and is still climbing, and companies and people are still flocking in. Big Japanese electronics firms in particular have established themselves as major employers. Toshiba Corp. alone has three large complexes and continues to expand.

Many say that UCI is at the center of the county's renaissance

American Electronics Association membership figures also help to tell the story: Orange County had 244 AEA members at the end of 1988, a 50% increase over the 1983 level and a steeper gain than any other part of California.

But it is UCI, with its campus in the center of the heaviest concentration of industry, that is the catalyst, according to Johnson and other top executives. Under chancellor Jack Peltason, the school has become much more than a supplier of well-prepared scientists and engineers from its top-notch departments in computer, electrical engineering, and biomedical sciences. The university acts as a dynamo for the area, county executives say.

PET PROJECT. Most top schools have programs that encourage the exchange of ideas and people between academia and area companies, but UCI has put extra emphasis on these since it started the push in earnest several years ago. A real winner is the Roundtable for Executives, one of Peltason's pet projects. Western Digital's Johnson, who heads the UCI board of trustees, believes it creates the kind of top-level forum lacking in the past where common issues and problems can be addressed.

"UCI has provided the new leadership for us to make the transition," agrees Carmelo J. Santoro, chief executive at Silicon Systems Inc. in Tustin. Since he arrived early in the decade, Santoro has been in the forefront of those working toward building this type of industry infrastructure. "[UCI] is playing the role that Stanford and Berkeley play [in Silicon Valley], with local research and support of technology," says Santoro, who has headed companies there and at other technology centers.

County-based executives credit Peltason, who assumed the chancellor's post in 1984, as the prime mover behind UCI's drive to fill the leadership void. His view is that the timing was opportune since before that Orange County technology firms "had not reached critical mass." Peltason, formerly president of the University of Illinois and dean of engineering at UCI, has lofty goals. He sees UCI's role for the region as nothing less than that of the cathedral in the Middle Ages, "where all life revolved around it."

Besides the UCI-sponsored Roundtable, the county has a less formal executive group called So/Cal/Ten (for Southern California Technology Executive Network) that since 1983 has helped fill the network void. When its members started holding early morning meetings to exchange ideas, it was the only networking game around, says Santoro. "Instead of drinks after work, we had breakfast. We created our own watering hole where we could talk and focus on problems."

Now there are seven separate roundtables with some 80 members within So/Cal/Ten, each holding monthly meetings, along with up to five conferences yearly.

VENTURE CAPITAL IS GETTING EASIER TO FIND

Venture capital, or rather the lack of local sources for it, has been a sore point for Orange County entrepreneurs through the years. "Managers who wanted to start a company mainly had to get on an airplane for San Francisco or New York," says Irvine capitalist Thomas Gephart. As managing partner of Ventana Fund, which was the county's first—it was founded in 1977—he is one of the few venture capital managers resident in these parts.

But the upswing in area fortunes is changing the startup financing picture. Gephart says that most of the major national venture outfits now make regular swings through Orange County, and some have opened offices. While his roots in the area still give Ventana an edge for scouting out new business, the competition for good deals is growing keener.

"It's clear that this is the place [venture capital and startup] people want to be," Gephart says. "It's really on an uptick." He counts more than 150 publicly owned electronics companies in the county, and says that privately held ones number many times that figure: some estimates of the total go above 1,000, but no one knows for certain.

Gephart's firm has some $140 million currently invested, much of it from overseas institutional and corporate sources. The strength of Orange County's high-tech industry comes from its wide diversification across military and most equipment categories, in his view. Therefore, when a recession or severe slowdown inevitably hits, "we're not entirely bulletproof—but mostly so." *—L. W.*

TASTE SOME OF THAT SWEET HIGH-TECH JUICE

Many of the industry executives active with UCI also take part in So/Cal/Ten, making up what is evolving into a county establishment, with the kind of clout establishment figures exert elsewhere.

In addition to Johnson and Santoro, prominent names include Gilbert F. Amelio of Rockwell International Corp., William P. Conlin of Anaheim's CalComp, and the cofounders of AST Research Inc., a leading personal computer manufacturer in Irvine, Safi U. Qureshey and Thomas C. K. Yuen. Among them, these firms tote up about $2.5 billion in yearly sales.

Among the new companies evolving in the county, there are signs of a distinctive character that sets them apart even from Los Angeles counterparts, just 50 miles to the north. Much of the growth is in small-systems companies, as opposed to components makers, which reflects the strong presence of giant military and aerospace suppliers. These include Rockwell International, Hughes Aircraft Co., and others, whose Orange County sites mushroomed during the buildup of the 1980s.

SYNERGY. Also, research in biomedical work at UCI is spawning a host of medical electronics companies that should make the area a national leader in the field. Such cross-pollination "mixes a combination of computer science, hardware, and software," says industry veteran Charles V. Kovac, a vice president of Rockwell's Communications Systems Group. Kovac, who has worked in the county for three decades, says the synergy started to happen when people "went across the street to see what's going on."

If any issue clouds the prospect of further smooth growth, it is the same one that dogs other parts of the Golden State. The inevitable consequences of the boom are the problems of soaring costs of facilities and housing along with gridlock traffic and other overcrowding. "It's a good area, but success comes at a stiff price," says David Methvin, founder of Computer Automation Inc. He is now with Davin Computer Corp., a three-year-old company that plans to produce 64-bit microcomputers. For example, a complex that Methvin leased for his company in Irvine for $2.75/ft^2 in the mid-1970s now goes for $25/ft^2. "Manufacturers have left for cheaper pastures," he says, which is the likely decision for Davin Computer when it's ready to start production.

Not only that, says Methvin, but "for some reason there hasn't been a core, so to speak." Lack of such a core, note Methvin and his fellows, held Orange County back in many ways, but particularly in the failure to spark the kind of establishment network of executives who make things happen. The advent of the Roundtable and So/Cal/Ten have gone a long way toward filling that gap.

Another obstacle is concern over potential pollution, making plant expansion difficult. For example, the community of Irvine objects to the use of certain chemicals at Western Digital's planned world-class submicron fabrication plant, and the plant's future is now in doubt.

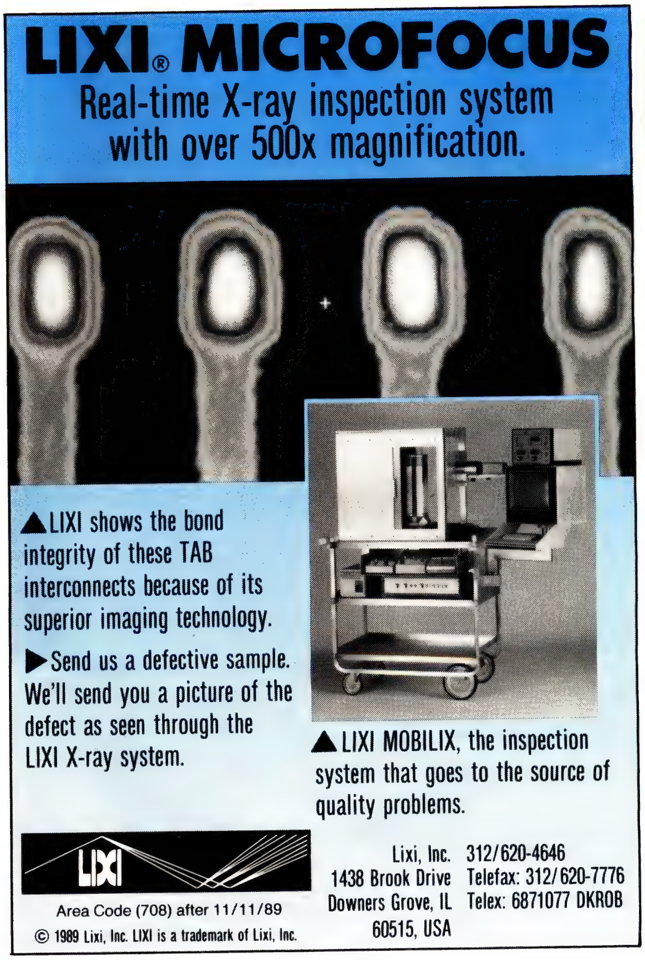
High real estate costs are a problem—some companies leave for cheaper pastures

Finding affordable housing presents a big challenge throughout the county, too, since its natural attractions of beaches and ideal climate have run prices to lofty levels. The median 1989 price of $251,600 for a home in Orange County is the second highest in the state, putting a purchase out of reach of 88% of households, according to recent studies.

These costs not only prevent most workers from moving close to the industrial complex near the central coast but also gives fits to companies trying to recruit engineers and executives. "It's very difficult to attract talent from elsewhere," admits AST Research cochairman Yuen. Conversely, once they settle in the area, few residents can be enticed away, Yuen adds.

Even Orange County enthusiasts like Santoro concede it likely that up to five years or so will be needed to digest recent growth. "The next jump is the most difficult—for 'Silicon Beach' to reach the size and content of Silicon Valley," he says.

But there is little question that the elements that have combined for today's growth in Orange County are still driving it powerfully. Observer Steve Panzer, a cofounder of So/Cal/Ten who has viewed the past five years from his Los Angeles base, speaks for the consensus. "There's something special about [Orange County], a dynamic feeling of optimism and innovation that has the sense of visiting the 21st century." *–Larry Waller*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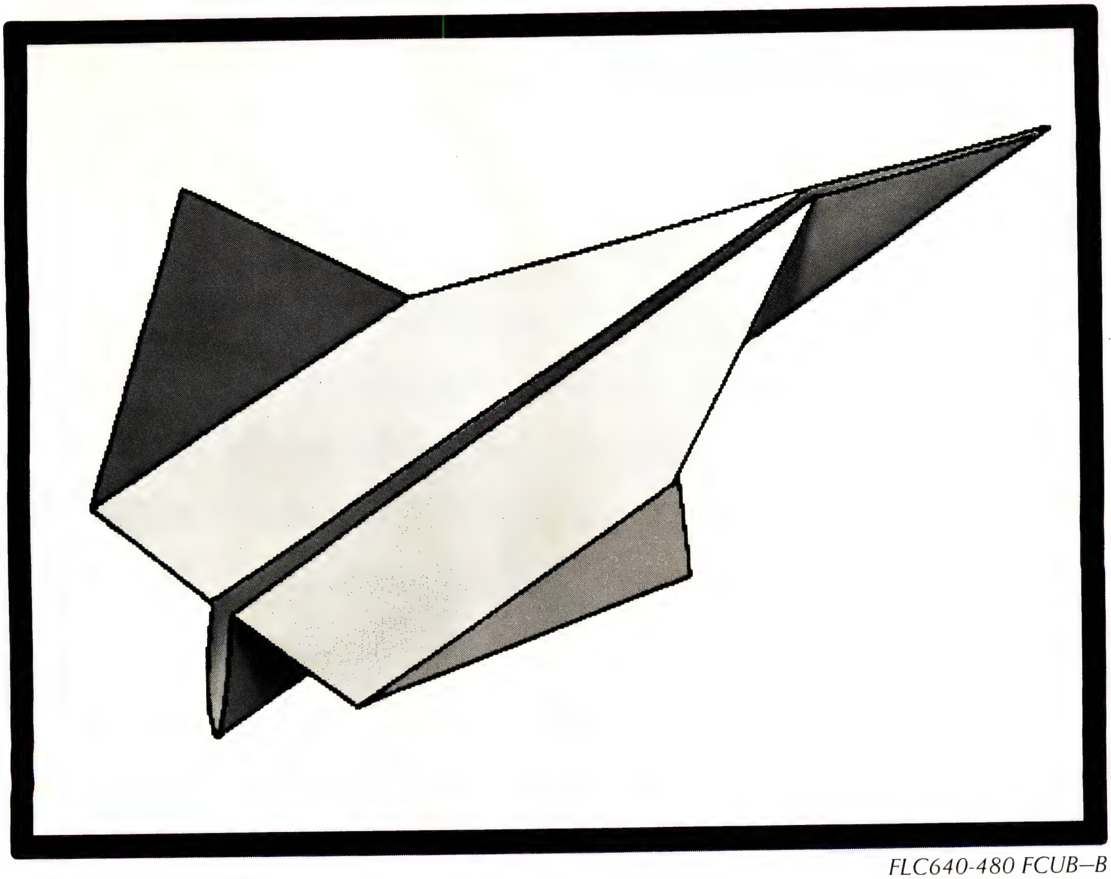

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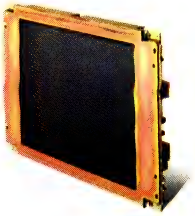

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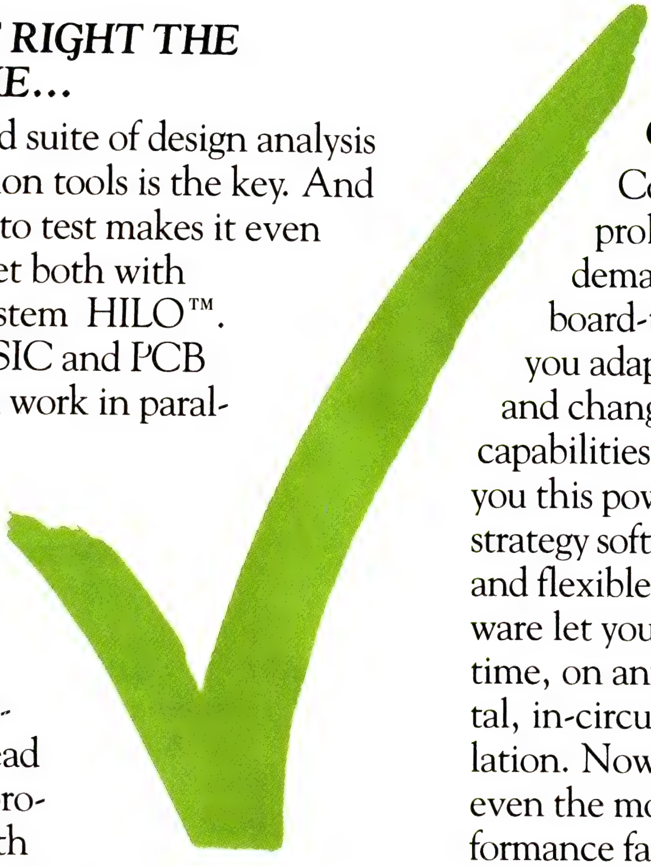

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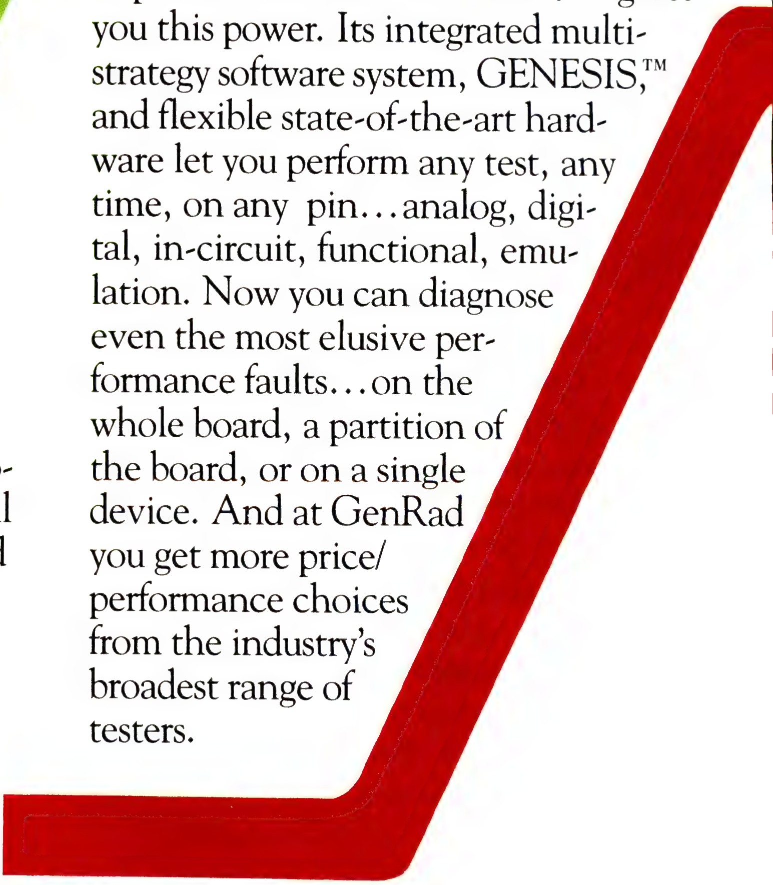

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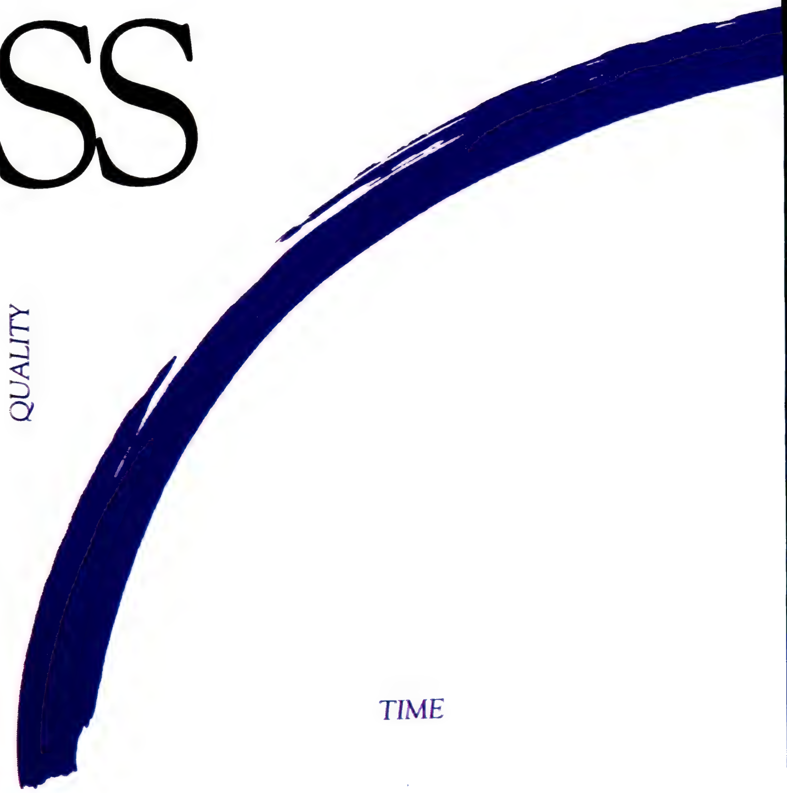

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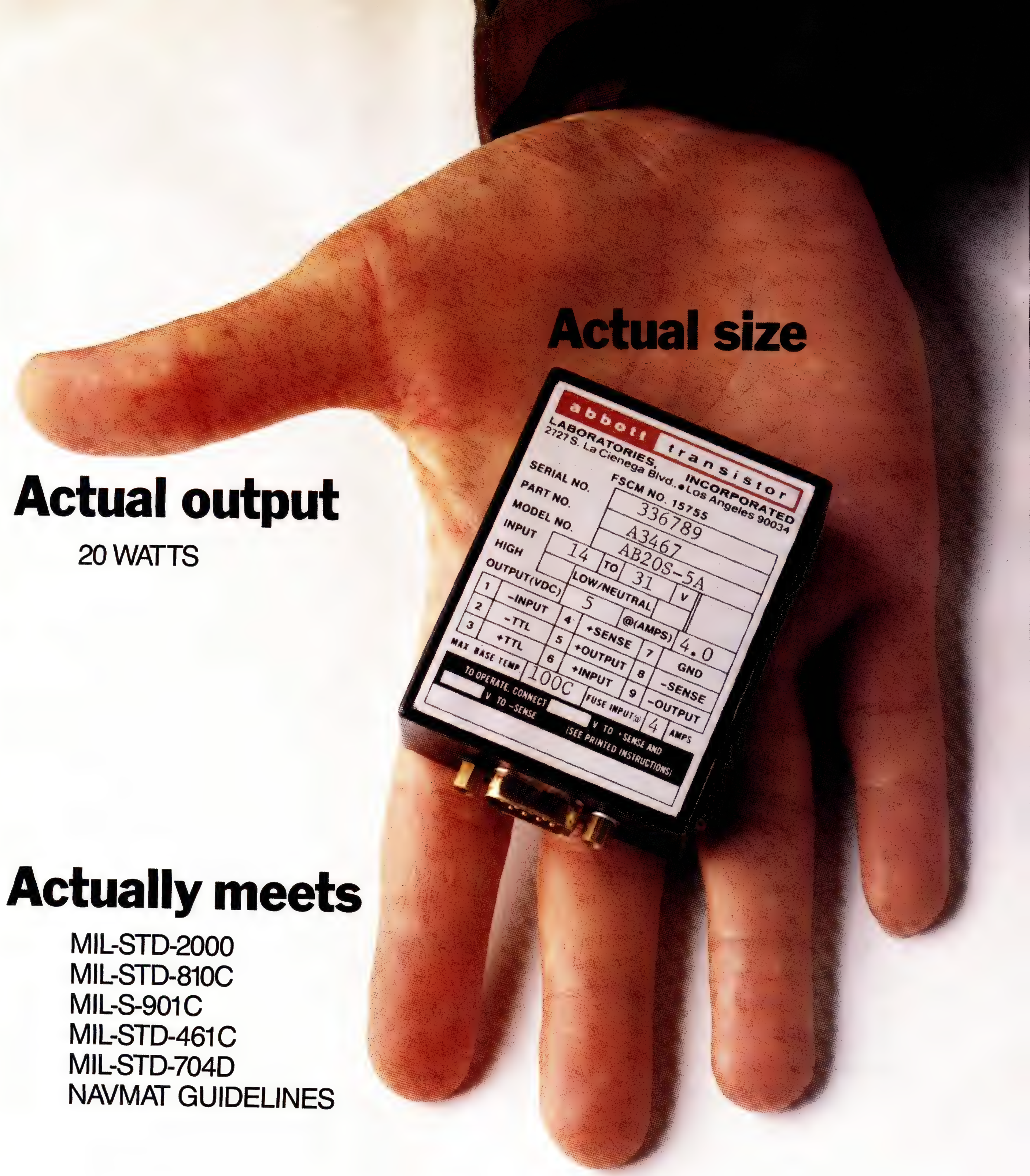

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ELECTRONICS NEWSLETTER

JAPAN CLOSES IN ON A PARALLEL INFERENCE MACHINE . . .

Eight years into the 10-year, $400 million Fifth Generation Computer Project, the Japanese appear close to coupling symbolic programming with advanced parallel-computing techniques. The project's core effort to build a Parallel Inference Machine with about 1,000 processors is on schedule, two to three years away from completion, say officials at Tokyo's Institute for New Generation Computer Technology (ICOT). Systems and software developed using ICOT's KL1 high-level logic programming language will be debugged on a 64-processor system in Tokyo. ICOT officials demonstrated a 16-processor version last month at Argonne National Laboratory in Argonne, Ill. But ICOT won't meet its goal of producing by 1992 a computer capable of reasoning. And natural-language comprehension won't come until after 1992, concedes Kazuhiro Fuchi, ICOT's managing director. □

. . . AS U.S. COMPANIES LEARN HOW TO SELL TECHNOLOGY IN JAPAN

The biggest reason that U. S. companies have trouble selling goods in Japan is inept marketing, says John P. Stern, vice president of Asian operations at the American Electronics Association's Tokyo office. Japanese government intervention and exclusionary business practices account for only part of the difficulties U. S. companies have in penetrating Japanese markets, Stern says. Many firms create their own obstacles, he says, by not positioning themselves to react quickly to new developments. For example, relatively few companies have branch offices in Japan. Without such a presence, it is nearly impossible to spot new markets soon enough, he says. Stern adds that those companies that buy goods in the Far East should station knowledgeable procurement officials there because Japan controls several industrial segments in the region. Companies doing business in Japan should also consider hiring a local public relations firm, he says. A local PR group may be able to head off the bashing in the Japanese press that many U. S. companies endure. □

IBM GETS READY TO UNLEASH ITS NEXT-GENERATION RISC PROCESSOR . . .

IBM Corp. is "close to production" on a second-generation reduced-instruction-set-computer processor, says John A. Armstrong, vice president of science and technology for IBM. Code-named America, the superscalar processor comprises six chips with a total of 6 million transistors and is built with the same 1.0-μm CMOS technology in IBM's 1-Mbit dynamic random-access memories. The chip set also contains a memory-instruction cache, a branch processor, a data cache, an integer chip, and a floating-point chip that meets the Institute of Electrical and Electronics Engineers standard for a 64-bit multiply and add operation. The processor, presumably to be used in IBM's RT PC work station, executes up to five instructions per clock cycle. □

. . . WHILE DEC'S VAX 9000 TAKES DEAD AIM AT IBM MAINFRAMES

Now that one of the worst-kept secrets in the computer business, the VAX 9000 from Digital Equipment Corp. of Maynard, Mass., has made its debut, DEC finally has a line of compatible computers and work stations to compete with mainframe kingpin IBM Corp. "from the desktop to the data center." The VAX 9000 outruns the original VAX-11/780 by 30 to 117 times, thanks to the use of scalar and vector processing. Of the more than 6,500 VAX software packages available for the VAX 9000, 80 are mainframe applications, including Computer Associates International Inc.'s Masterpiece II financial-management software. The VAX 9000 with the VMS operating system will ship in the second quarter of next year; DEC's version of Unix, Ultrix, will be available for the 9000 in the fourth quarter of 1990. □

ELECTRONICS NEWSLETTER

HP'S TEAM COMPUTING MAKES MULTIVENDOR NETWORKING EASIER

With Team Computing software from Hewlett-Packard Co., customers can link computers from different vendors in a way that converts a network into a distributed supercomputer, says the Palo Alto, Calif., company. The Task Broker component employs intelligent bidding to distribute an entire task to the networked computer that's best suited to execute the job. Task Broker runs on any Unix computer and uses the TCP/IP protocol. Other key elements are the Network Computing System pioneered by HP's Apollo Division, the X-Window graphical interface developed by the Massachusetts Institute of Technology, and the Motif user interface developed for the Open Software Foundation by HP and Digital Equipment Corp. Team Computing software will be available in January to link computers using NCS, which has been licensed by more than 200 companies, including Apollo, Convex, DEC, HP, IBM, Multiflow, Prime, and Sun. ☐

INTEL-ALLIANT STANDARD SPURS 860 IN PARALLEL COMPUTING

The Intel i860 microprocessor should be even more attractive for parallel-computing applications thanks to an agreement on a software standard between Intel Corp. of Santa Clara, Calif., and Alliant Computer Systems Corp. of Littleton, Mass. The Parallel Architecture Extended (PAX) standard, an extension to the existing binary standard for the i860, consists of hardware and software engineering rules that allow developers of i860-based systems to apply multiple parallel processors to a task. With PAX, software developers can write one version of code that runs on platforms ranging from work stations to large shared-memory parallel processors. Under the agreement, Intel will incorporate PAX-standard code in future generations of the i860; Alliant will license its automatic parallel compilers and graphics technologies to Intel for use by other customers developing i860 CPU-based machines. ☐

AT&T AND DU PONT TEAM UP TO PUSH A METRIC CONNECTOR STANDARD

One of the last bastions of English measurement in electronics—connector technology—is under attack by a powerful duo. Following the lead of the recently adopted IEEE Futurebus Plus standard, which calls for a metric interconnection, AT&T Microelectronics and Du Pont Electronics are pushing a new, high-density interconnection system called Metral as a world standard for telecommunications, data-processing, instrumentation, and industrial markets. The Metral system is based on a 2-mm grid; it provides up to 432 signal positions on a double-high Euroboard—more than twice the 192 positions available with present-generation DIN connectors. AT&T Microelectronics of Berkeley Heights, N. J., and Du Pont Electronics of Wilmington, Del., will jointly develop Metral products, but they will manufacture and market the products separately. The first offerings will be available in January. ☐

U. S. MEMORIES SETS ITS SIGHTS EVEN HIGHER

Look for the U. S. Memories Inc. bandwagon to pick up steam again after its revised and more aggressive business plan is circulated early this month among the seven original consortium members and several potential new ones. The dynamic random-access-memory consortium's plans call for "a significantly larger facility in terms of output than originally conceived," says Sanford Kane, U. S. Memories' president. Migrating from IBM's 4-Mbit to its 16-Mbit DRAM technology inside the yet-to-be constructed fab is a key element in the revised plan. Kane expects two major companies to sign on with U. S. Memories "within a couple of weeks" after the plan is distributed; visits to prospective fab sites will begin this month. ☐

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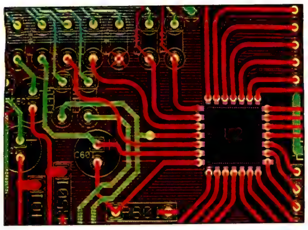
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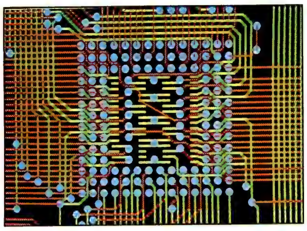
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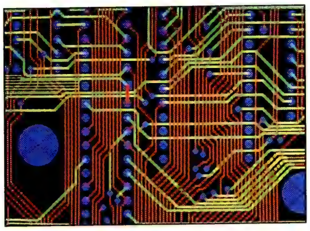
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Circle 142

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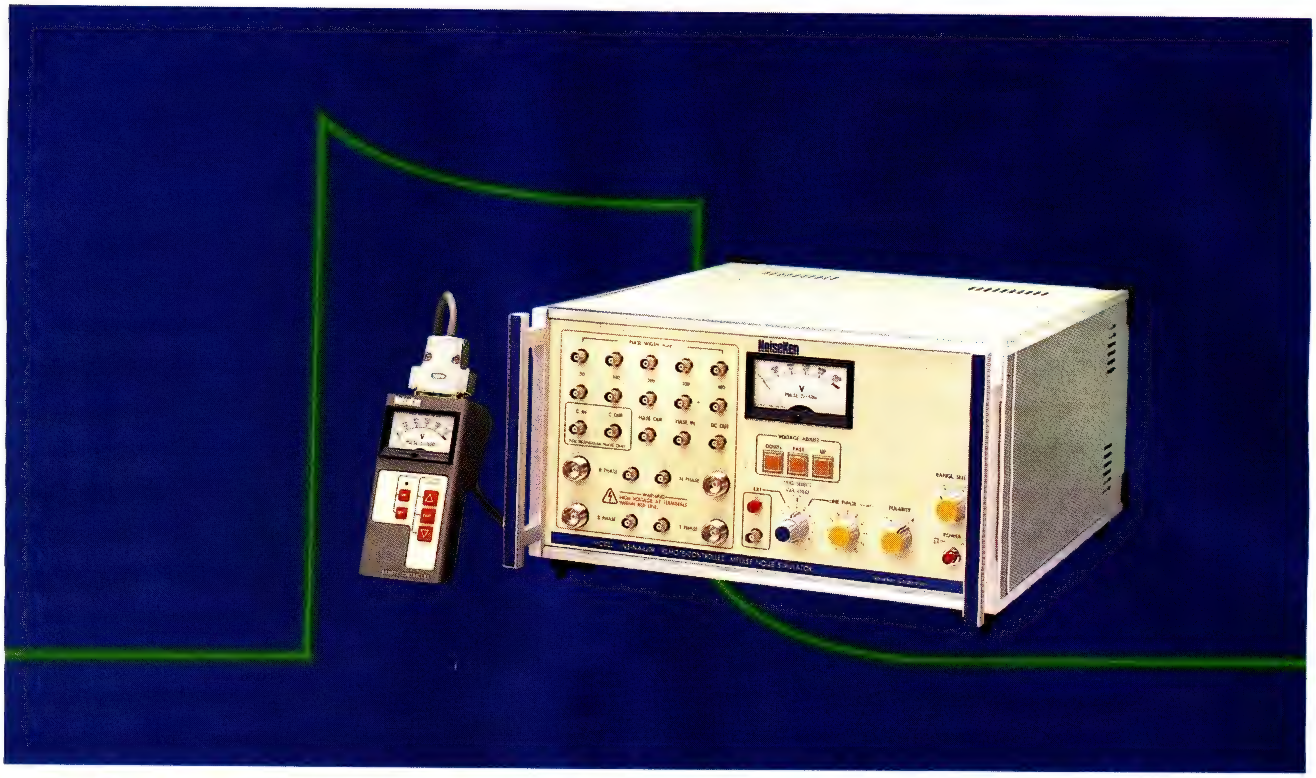

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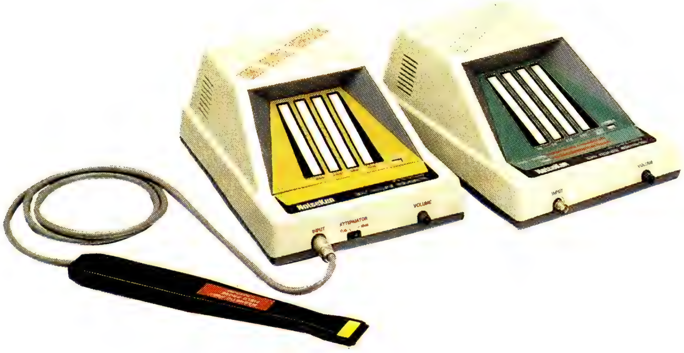

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Circle 286

PRODUCTS TO WATCH

SILICON GRAPHICS OPENS ITS GRAPHICS LIBRARY TO THIRD-PARTY VENDORS

In a move that will speed industry adoption of both 3-d graphics visualization technology and high-speed networking, Silicon Graphics Inc. of Mountain View, Calif., has unbundled its Distributed Graphics Library source code from its Iris hardware platforms. DGL can now be implemented on any system running Unix System V Release 3 or Unix BSD 4.3 with a standard-sockets interface. Reference ports are available for other Unix implementations, including IBM Corp.'s AIX running on IBM 3090 mainframes and Digital Equipment Corp.'s Ultrix. Interfaces are also available for computers from Alliant, Connection Machine, and Cray Research. Networking can be implemented using TCP/IP over Ethernet, but Silicon Graphics is committed to state-of-the-art networking products such as the Fiber Distributed Data Interface. Available now, DGL source code is priced at $5,000 per host. □

HP INTEGRATES LOW-COST X-WINDOW TERMINALS INTO ITS WORK STATION LINE

With prices starting at $3,000, the HP 700/X family of X-Window graphics terminals addresses the low-end market segment in the Palo Alto, Calif., company's work station offerings. The terminals deliver the same graphics and local-area-network performance as a $6,000 entry-level work station configured as an X server in the X-Window System developed at the Massachusetts Institute of Technology. Available in a range of color and monochrome options, the 700/X family can be packaged in mechanical or electric design stations, computer-aided software-engineering work stations, and industrial applications in which users must display multiple process windows. They come with 1 to 4 Mbytes of dynamic random-access memory and can support 16 colors from a palette of 4,096 colors or 16 levels of gray scale. Graphics output and X-Window support are controlled by a 50-MHz Texas Instruments Inc. TM34010 graphics chip. □

INTEL PUSHES ITS REAL-TIME OPERATING SYSTEM TO 32 BITS

Real-time applications running on Intel Corp.'s 32-bit microprocessors that are bogged down by the company's present 16-bit iRMX II real-time operating system can realize significant performance gains now that Intel's OEM Modular Systems Operation in Hillsboro, Ore., has released the 32-bit iRMX III operating system. Since iRMX III is binary-compatible with its predecessor, 16-bit applications can run concurrently with 32-bit code, enabling 16- and 32-bit tasks to communicate with each other. iRMX III also supports Intel's protected mode, which makes debugging of development programs easier and allows for addressing of up to 4 Gbytes of memory. A single copy of iRMX III costs $5,650. Run-time licenses are also available. □

HARRIS'S 80C286 BEATS THE COMPETITION TO THE PUNCH ON MIL-STD-883

Portable military instrumentation, avionics, and weapons systems based on Intel Corp. microprocessor architectures can now migrate to an 80286 CPU with a new chip from Harris Corp. The 80C286/883 lays claim to being the first CMOS 80286 microprocessor to meet the Class B electrical, mechanical, life, and packaging requirements of MIL-STD-883. Harris's Semiconductor Sector in Melbourne, Fla., is offering 10- and 12.5-MHz versions of the device. Commercial CMOS versions of the 80286 are available from Intel and Advanced Micro Devices Inc., but Harris is first to meet the "shake, rattle, and roll" and extended-temperature range (–55° to +125°C) demanded for 883 qualification. Housed in a 68-lead pin-grid-array package, the device is available 16 weeks after ordering. The 10-MHz part sells for $604 each in quantities of 100; the 12.5-MHz unit is priced at $714. □

PRODUCTS TO WATCH

SPACE-SAVING BURN-IN UNIT HEATS WITH HIGH-FREQUENCY CONDUCTIVE TECHNIQUE

A novel semiconductor burn-in system applies high-frequency conductive heat directly to a device's case instead of using large convection ovens or liquid burn-in systems. Called Bak Pak by developer *EJ Systems Inc.* of Lawrence, Mass., it fits on a desktop and can deliver temperatures of up to 200°C. Heating is controlled by using an MS-DOS personal computer to drive individual microprocessors at each heating position. The chips maintain each device's case temperature to within ±2°C. Drive electronics on each burn-in board provide good signal quality at up to 40 MHz, the company says. Each burn-in module has four 23.4-by-9.1-in. burn-in boards, each with four heating positions. Bak Pak sizes range from 16 to 500 positions. Prices range from \$10,000 to \$50,000; delivery is eight weeks after ordering. ☐

GREENWICH INSTRUMENTS' 1-MBIT RAM BOASTS 20-YEAR BATTERY BACKUP

Configured as 128 Kbits by 8 bits, the GR12882 from Greenwich Instruments USA Inc. uses a high-reliability lithium power cell for its backup power and features fast power-down circuitry to conserve power and data. The circuit is referenced at 4.5 V and can switch to battery backup in 15 μs. After the system powers down, the GR12882 can be transported to another system, which makes it ideal for data collection, program development, and program changes in process control, automation, robotics, and user-definable lookup tables. The Charlotte, N. C.-based company has put the chip and its battery into a package that measures 0.45 in. high, 1.8 in. long, and 0.7 in. wide. It is a follow-on to the company's line of lower-density nonvolatile RAMs, including a 256-Kbit chip. Available now, the GR12882 is priced at \$187 each in 100-unit quantities. ☐

SIEMENS ISDN TRANSCEIVER CHIP HANDLES U. S. LINE CODE

Siemens AG is dishing up the first CMOS single-chip solution to echo compensation on integrated services digital networks that use the North American 2B1Q line code. The West German chip maker's PEB2091 uses a special digital signal processor integrated on-chip to compensate for echoes on two-wire ISDN U-interface lines between the subscriber terminal and the phone company's central switch. Suitable for all exchanges and terminals in countries subscribing to American National Standards Institute rules, the 2091 distinguishes between the two transmission points and also reduces noise on the line. By exploiting all CMOS design possibilities, the chip limits its power demands to 300 mW. The 2091 is available now in 44-pin ceramic packages and is priced at \$60 each in 5,000-unit quantities. ☐

RADIX DEVELOPMENT TOOLS FOR VMEBUS CUT DESIGN CYCLE TIME IN HALF

A new generation of single-board computers complete with system development tools is drastically cutting the time required for VMEbus board-level system design. Radix Microsystems Inc. claims its EPC-3 hardware and EPConnect VMEbus software-support package reduce design cycles from 18 months to just 6 months in some instances. Based on Intel Corp.'s 80386SX microprocessor, the EPC-3 board fits into a single VME slot and integrates the primary functions of an embedded personal computer. The Beaverton, Ore., company's board includes the CPU, up to 4 Mbytes of dynamic random-access memory, a numerical coprocessor, serial and parallel I/O, keyboard interface, and a VGA graphics controller. For more flexibility, Radix has developed a new bus that is electrically similar to the PC AT bus but allows two expansion modules per VMEbus slot. Many storage and I/O options are available. Pricing starts at \$2,595 per module. ☐

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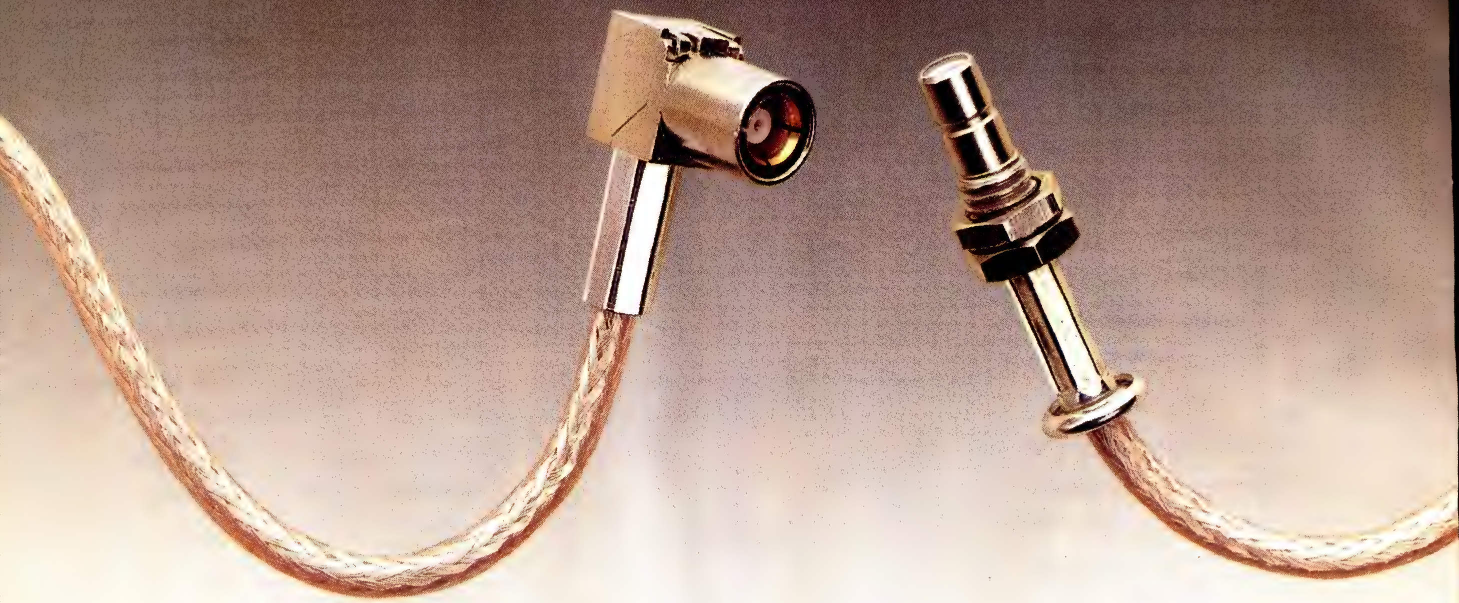

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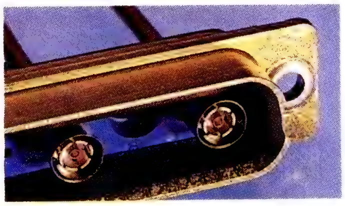

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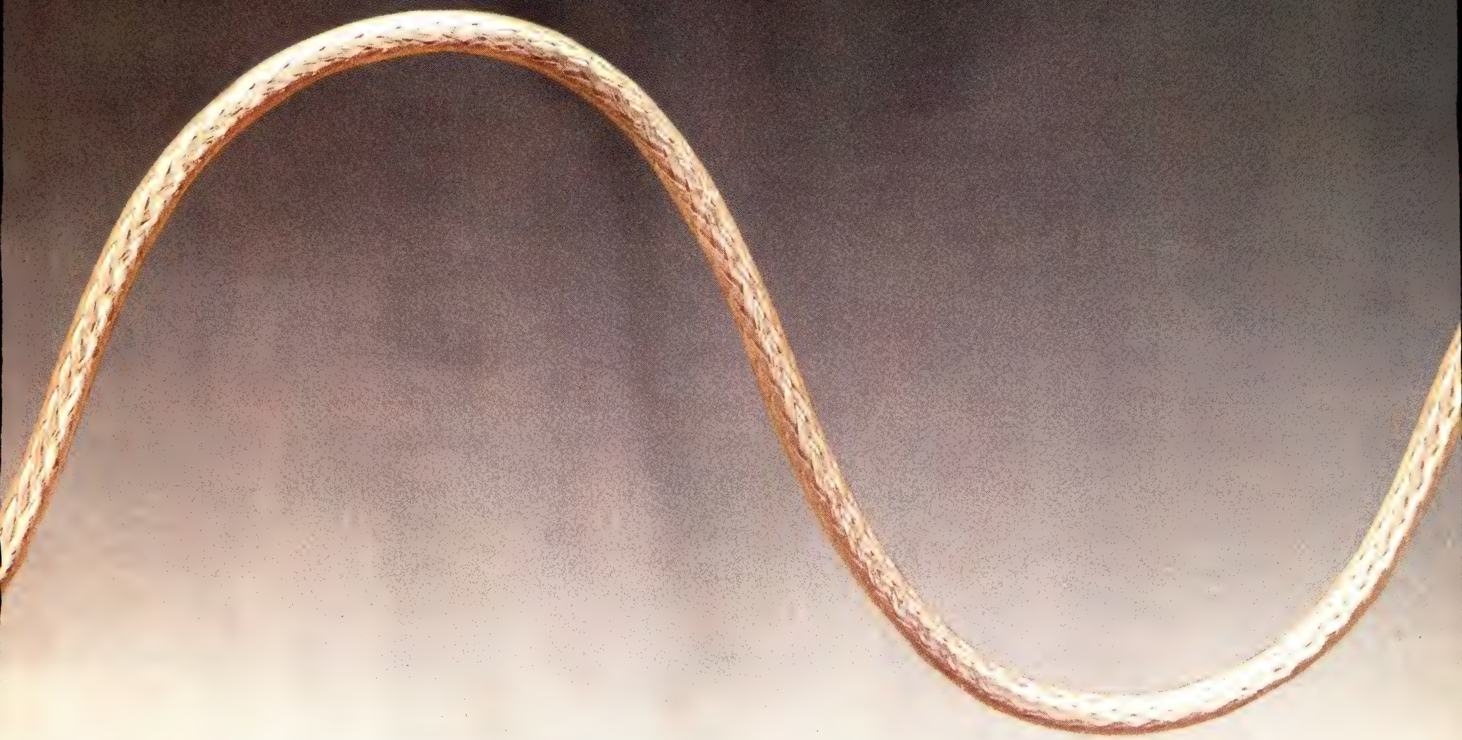

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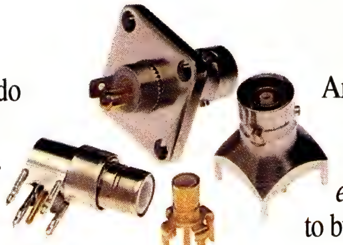

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Circle 234

DEFENSE FIRMS FACE THE MUSIC: IT'S NOT GOING TO GET BETTER

EIA's 10-year forecast sees 2% annual drop through 1994, flat after that

LOS ANGELES

Faced with business prospects from their dominant customer—the U. S. government—that keep looking grimmer, defense electronics manufacturers still are trying to get a good grip on them. From all indications, it isn't easy: many companies agree that conditions are worsening—but not for them.

That's the seeming contradiction that emerges on the heels of the 25th annual 10-year forecast on defense spending from the Electronic Industries Association. The forecast, which typically gets high marks from the industry for its accuracy and no-nonsense conclusions, predicts decreases averaging 2% a year through 1994, and a flat market for the remaining five years. Though the numbers are only slightly more pessimistic than last year's, the predictions are more qualified and sprinkled with caveats reflecting much uncertainty.

TOO OPTIMISTIC? Many of the more than 300 industry representatives attending the Los Angeles meeting last month at which the report was introduced said it is "way too optimistic," in the words of one veteran military marketing executive. In their opinion, the predicted 2% annual drop understates what will prove to be much deeper cuts caused by budget constraints and arms-control agreements. But these same executives for the most part think their own companies' pieces of the Pentagon pie will not be cut.

Why the disparity? It can be explained best by taking a look at the EIA's prediction of a Department of Defense budget for fiscal 1990 (the year that began Oct. 1) of $295.6 billion. That figure—as yet unapproved—is a far cry from the Reagan Administration's projected $479 billion for that year, a request made in 1986 to pay for all the programs then on the books. But despite intervening budget cuts, many defense electronics firms have continued to base their plans on the earlier, higher levels of spending and only recently have started to face reality.

The "it can't happen here" view makes little sense to observers such as Lawrence Harris, aerospace and electronics financial analyst at Bateman Eichler Hill Richards in Los Angeles, a regional brokerage house. But it may be changing.

Harris notes that his industry contacts already have cranked down their internal forecasts from a year ago, "when they expected to grow 10% a year. Their opinion was that it's the other guy's programs in jeopardy," he says. By next year, he adds, company forecasts and overall market prospects should converge toward the downside as events unfold.

By then, already heavy pressure for cuts will be stepped up further, especially from Congress, forcing more belt-tightening by military customers. It will then become clear that contractors will have to go all out just to hold on to current business, much less latch on to the few new programs coming on stream.

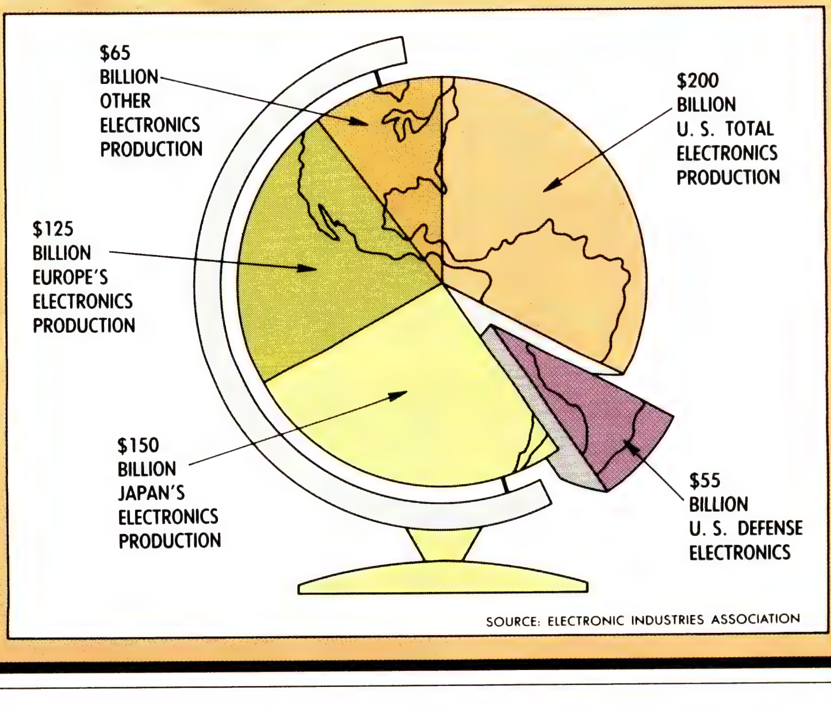
"Hard choices will have to be made," says EIA forecast chairman Geoffrey K. Bentley. "It will not be business as usual." Adds one industry player: "Over the next 10 years we will return to spending levels, in real terms, last seen in 1981."

Still, there are opportunities in defense electronics, the study points out. Of the some $1.1 trillion expected to be spent by the DOD in the coming decade, electronics will get more than $500 billion, according to the forecast. And in several hardware categories, real growth (adjusted for inflation) can occur. The clear winners will be space equipment, along with electronics and communications hardware, which are slated for spending increases.

DOUBLE RISE. The way the forecast sees it, spending for space-based procurement and RDT&E—research, development, test, and evaluation—as well as for electronics and communications will rise in both real dollars and percent share of the total, the only categories for which that will be the case. By comparison, such classifications as aircraft, missiles, and ships will drop in terms of real dollar growth in the near future.

The expected increase for space-based RDT&E plus procurement will be $11.7 billion in fiscal 1999, compared with $10.5 billion in fiscal 1990. For electronics and communications, the figures will be $11 billion and $10.2 billion for those same

A BIG SLICE OF THE WORLD PIE



SOURCE: ELECTRONIC INDUSTRIES ASSOCIATION years, according to the EIA study.

One irony is that a major reason for lowered defense spending—arms-control agreements—also spurs the electronics portion. That's because the pacts bring with them heightened need for surveillance and verification hardware, which is rich in electronics.

Also interesting in the new forecast is the continued retreat of the once prominent Strategic Defense Initiative. This year the decline in Star Wars fortunes relegates it to routine treatment as just another "high-tech research program" without a specific forecast.

Another major shift is in the key RDT&E portion of the budget. In the past, RDT&E was heavily skewed to projects that were far in the future. Total spending will stay about the same, says the EIA, but it will be reoriented toward more immediate "force-multiplier or high-leverage payoffs." As examples, Bentley offers systems with high electronic content such as self-guided smart weapons, unmanned vehicles, and antisubmarine-warfare equipment.

Programs backed by the Pentagon with commercial fallout also are getting more support. Among them are artificial intelligence, high-definition TV, and the Sematech venture for improving semiconductor manufacturing technology.

The bottom line to all the changes envisioned by the EIA is that those in the business face their stiffest challenge ever, says analyst Harris. "To survive," he advises, "they must be nimble and judicious in how they balance their outlays." The trick is to plow investment into R&D that can apply to many potential programs and hold back capital investment unless there is a sure payoff.

FIND A MATCH. At least one player in the field, TRW Inc., has been pursuing such a course since the crunch began in 1986, says John Mellen, its director of strategic planning and analysis. "What we try to do is identify those areas [defense electronics programs] that hold up and match up with our capabilities," he says.

Right now, those include command and control gear, integrated avionics packages, and antisub warfare. TRW's Redondo Beach, Calif., Space and Defense Sector, with annual sales of about $3 billion, has programs in all these areas and is seeking more.

Mellen says TRW uses the EIA forecast as a basis for its own planning, since "historically it has been good." He believes predictions for the next two fiscal years are "about right," but things get cloudier after that. Defense spending trends "never have gone the same way for more than five or six years, and we're already more than three years into this one," he says.

Harris doubts that even fiscal 1991 will stay on the forecast track because the details of arms-control agreements cannot be foreseen. At the very least, the mix of U. S. forces will change drastically, he says. The consequences of such changes will be severe for companies that supply the equipment for programs that are curtailed.

But Harris does not share the EIA's conclusion that major programs will not be eliminated outright in 1990's budget to reach 1991 defense budget goals. Big spending jumps are in the offing for heavyweight projects such as the B-2 bomber, Mil-Star satellites, the Advanced Tactical Fighter, and the Advanced Tactical Aircraft.

Some observers, including Harris, believe that one or more of these high-visibility efforts must go to pay for more mundane, but critical, tasks. However, the EIA thinks that cutbacks and trimming will do the job. "From my perspective, the outlook is very uncertain," he says, "and companies must take that into account."

–Larry Waller

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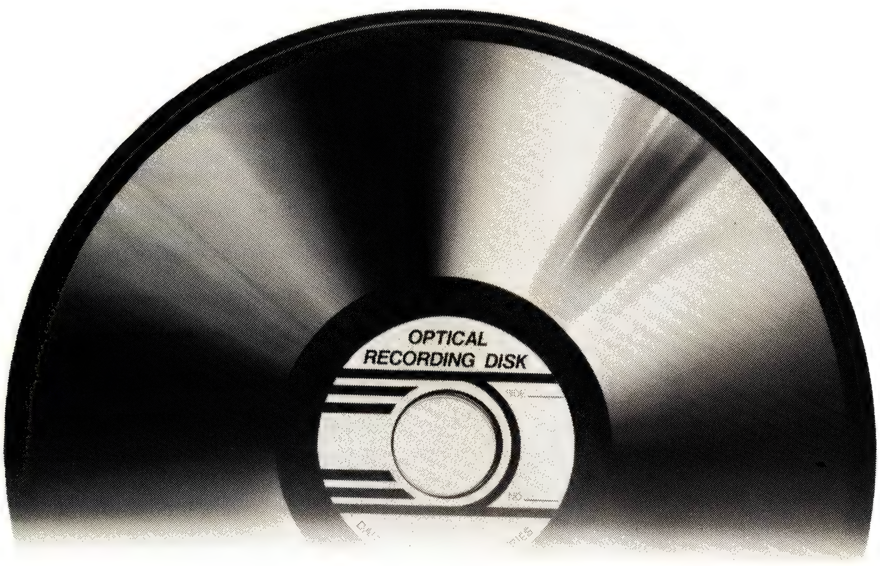

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Circle 406

THE EARTHQUAKE

ALL IN ALL, FOR THE VALLEY IT COULD HAVE BEEN WORSE

SAN JOSE, CALIF.

The damage suffered by Silicon Valley electronics manufacturers in the Oct. 17 earthquake can be measured on two levels. One is equipment: there, in most cases, companies came through fairly well with only minimal disruption. But on the other level—people—the disruption caused by the great quake of '89 was both immediate and long term.

In the days after the quake, the visible signs of disarray came in the form of employees unable or unwilling to make the trek to the office. Oct. 18, a Wednesday, became an unofficial holiday. The employees who did come to work found half-filled parking lots and office space strewn with debris.

It was as if a group of revelers had entered buildings and trashed each office, throwing papers and belongings in aisles, capriciously moving furniture and room dividers askew, and pulling light fixtures and false ceilings from their moorings, scattering them about the floor. Those making it to work spent the day after assessing the damage, videotaping the results to document them for insurance purposes, and putting things back together.

> Equipment and offices were damaged; workers couldn't get there

In offices, the significance of the phrase "backing of the hard disks" also became glaringly obvious. The experience of Dave Purvis, engineering service manager at Versatec Inc. in Santa Clara, illustrates the point dramatically. He says local-area-network file servers in his building danced about the floor during the quake. "After the shaking stopped," he says, "they failed to come back on-line."

FILE SERVERS DOWN. The network has 10 file servers serving several hundred users. The network, down on Wednesday, was fully functional on Thursday except for the file servers. "You could access files stored at individual work stations and use the print servers, but you could not access any data on the file servers," Purvis says. "The servers were backed up, but some data that missed the incremental backup could have been lost."

At 3Com Corp., the Santa Clara manufacturer of LANs, the company's own wide-area network, which provides national and international electronic mail for all company facilities, was not damaged. It was down briefly due to power outage during the earthquake, says company spokesman Norman Lambino, but when power came back the network resumed operation without any serious disruption.

None of the 60 computer systems at Tandem Computers Inc. in Cupertino, which makes fault-tolerant computers, were damaged, although many lost power and shut down. Battery packs allowed them to fail softly. When power was restored, the systems resumed operation with no data loss.

MOTIONLESS MONEY. The earthquake also affected financial institutions. Immediately after the quake, many automatic teller machines were shut down. While that affected large numbers of small depositors, larger customers were also put out. James Adkisson, vice president of marketing at Insite Corp. in Milpitas, says a round of venture financing his company was negotiating and had planned to close that week was delayed because Insite's bank was unable to make the large-scale electronic funds transfers that were required.

Semiconductor production facilities had some problems. Those that survived the shaking with minimal damage were affected more severely by the loss of power in the aftermath of the quake. A fab out of power for several hours runs the risk of a contaminated clean room, says Mark Allen, vice president of manufacturing at Cypress Semiconductor Corp. in San Jose.

Meanwhile, grapevine talk among fabrication workers gathering around the lunch wagons for coffee break was of damage within the production facilities.

One tells the story of a computer tipping over and shutting down the line and of workers struggling to right the behemoth. Another tells how the earth tremors tipped over and scattered "box stock"—finished goods, sorted into various product grades—all over the floor. Parts that hit the floor had to be retested.

Besides semiconductor facilities, other companies in the Santa Clara Valley were down for various reasons. Broken water lines that flooded several buildings caused IBM Corp. to close its South San Jose facility for more than a day. Disk-drive manufacturer Maxtor Corp. in San Jose suspended operations to permit repair of power lines dislodged by the shaking.

Maxtor rival Seagate Technology Inc. in Scotts Valley, near the quake's epicenter, closed down for a couple of days, but managed to ship products from its Columbus, Ohio, facility. Company management worked at home, doing business via telephone and fax machine. *–Jonah McLeod*

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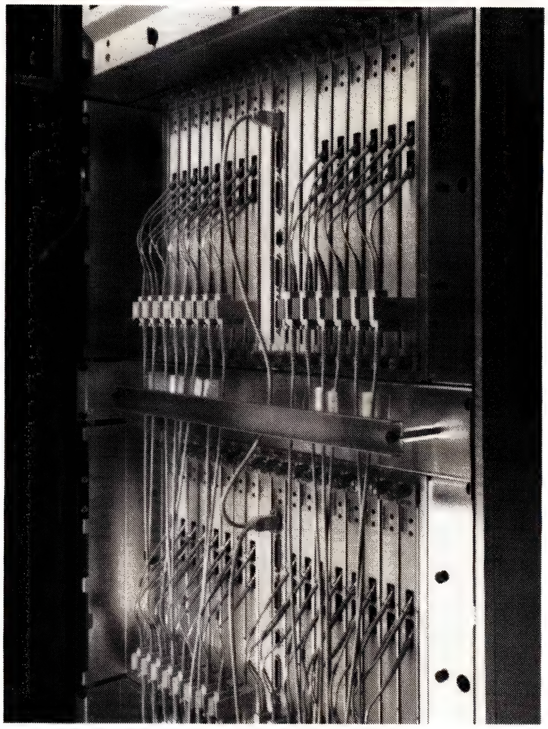
TANDEM'S CYCLONE BLOWS AWAY THE REST

CUPERTINO, CALIF.

In the on-line transaction-processing market, Tandem Computers Inc. has long held sway. Now the Cupertino company has made a move that gives it such a formidable lead in that business that only the likes of IBM Corp. can effectively challenge it.

Tandem's new high-end Nonstop Cyclone system, announced last month, extends the performance range of the company's product line by a factor of five. That rise inspires one observer to liken the company to a surfer on a wave that is turning into a tsunami.

According to Joseph Payne, an investment analyst with Alex. Brown & Sons in Baltimore, the $5 billion OLTP market is growing at 10% to 20% per year and could go even higher. It is split between IBM, which serves the transportation industry, and Tandem, which serves banks with such systems as automatic teller machines. The appeal of on-line systems is simple, says Robert T. Jolis, vice president of product marketing at Tandem. "It costs $1.25 for a teller to process a transaction, whereas on an automatic teller machine it costs 25 cents."



Nonstop Cyclone boasts a superscalar architecture that allows it to run two instructions per clock cycle.

Payne believes OLTP is growing into a broader market called on-line enterprise computing, a category that encompasses many more traditional data-processing applications. He says this market can achieve 20% to 30% growth to become a $20 billion segment by 1995.

Tandem's Cyclone puts it into an enviable position to exploit this broader market by providing higher initial computing power and greater expansion capability over the company's existing VLX system. Nonstop Cyclone performs three to five times better than VLX, which was introduced in 1986, says Joe Bennington, product manager at Tandem. The VLX, for its part, offered twice the performance of Tandem's earlier Nonstop system. Cyclone's performance puts it in competition with IBM's 3090 mainframes.

Tandem achieves this feat with new semiconductor technology and a new architecture. Bennington says application-specific emitter-coupled-logic devices are used in critical circuits such as cache and arithmetic logic units, while TTL is used in the communications-bus-control logic. And CMOS is used for faster static random-access-memory storage arrays. These high-speed SRAMs help drop the average memory cycle to 45 ns from the VLX's 83 ns.

Moreover, the system's new superscalar architecture allows two instructions per clock cycle, the first commercial mainframe system to do so, claims Bennington. Data and instruction words have separate paths to memory, a scheme that affords a 1.8 times improvement in performance over the VLX.

Cyclone also has a dual two-stage prefetch pipeline and a dual six-stage execution pipeline. Up to 16 instructions can be in some stage of execution simultaneously. To make the most efficient use of the pipelines, the system has a branch-prediction algorithm that successfully anticipates the outcome of a branch instruction 90% of the time. That saves six clock cycles.

FIBER LINKS. Another distinctive feature is the Dynabus, a fiber-optic link up to 50 meters long that connects processors. With Dynabus, processors need not be butted in order to share a common high-speed communications bus. Fiber-optic links of up to 100 and 500 meters also connect disk drive and communications subsystems, respectively, to processors.

The fiber-optic ties allow processors and peripherals to be physically separated and still maintain high-speed processor-to-processor communications. This is an important feature for facilities managers who require maximum flexibility in placing computer equipment in expensive computer-room space.

One big question is how, in a world where standard computer architectures and standard operating systems have become the rule, Tandem can roll out a new system that uses a proprietary operating system and hardware. The answer is that Tandem's operating system gives it a tightly integrated environment for relational data-base processing, says Peter Burris, director of IBM research at International Data Corp., the Framingham, Mass., market watcher. And it offers enough benefits that customers are willing to accept its being proprietary.

In Burris's view, Tandem's only competitor is IBM. Payne of Alex. Brown includes Digital Equipment Corp. as well. According to Burris, Tandem is selling its on-line product into two markets: against mainframes other than IBM's, and to IBM customers that are switching from Big Blue's Information Management System and VSAM (virtual storage access method) flat-file structure to a relational structure such as IBM's DB2.

In a recent head-to-head clash between IBM and Tandem, the latter won hands down. The competition was for a $5 million contract from the California Department of Motor Vehicles. As part of the competition, the DMV prepared a set of six tests that represented the typical processing it required.

IBM's solution was a 3090-400S-class system containing four processors. It passed only one of the six tests in the suite. Tandem passed all six tests using a system comprising 28 VLX processors. In September, Codd and Date Inc., a San Jose, Calif., consulting group, reran the suite using a Tandem system containing five Cyclone central processing units. The configuration aced the test; as a result, the DMV is considering using Cyclones instead of VLXs.

On the DEC front, says Payne, the competition comes from the Maynard, Mass., company's newly announced VAX 9000 series, which will be aimed at transaction-processing applications. The first VAX 9000s are slated to roll out next spring. Initially, the 9000 will have two processors, eventually going to four. Each processor will cost approximately $1 million.

Starting price of a four-processor Cyclone is $1.995 million; the top-end 16-processor system is $9.995 million. Limited quantities are available now, and production volumes will be available by the end of this year. *–Jonah McLeod*

A PERSPECTIVE ON ASIC DESIGN

"At Texas Instruments, you have the choices you need to get the ASIC you need. That's the difference between an ASIC device and an ASIC solution."

"An ASIC solution is more than a choice of silicon. To keep you from compromising on a square peg for a round hole, an ASIC solution involves many considerations: Your performance needs. How much control you want to exercise. The amount of support you require. What you can spend. How narrow your market window is. It's the result of you and your supplier weighing all the choices and reaching a balanced decision. At Texas Instruments, that's the way we like to work.

"A solution should not limit you to 'classic' ASICs — gate arrays and standard cells. That's why TI includes user programmables in its ASIC lineup. We manufacture high-performance, programmable logic devices (PLDs) and high-density, field-programmable gate arrays (FPGAs).

"Such a broad choice allows you to make better value judgments about control, NRE investment, and cycle times.

"TI advocates open-system CAD architectures instead of confining you to proprietary CAD systems. We support both PC- and workstation-based design systems.

"We provide as much advice and counsel as you need or want just about anywhere in the world. Our documentation is so comprehensive it can fill your bookcase as it fills your needs.

"We are looking to future solutions. For example, we are developing submicron CMOS and BiCMOS gate arrays and standard cells with densities over 100K gates. We are extending our support by developing software that migrates FPGA designs to mask-programmed gate arrays.

"An ASIC solution also brings with it assurances of the supplier's dependability, stability, and capability to produce and deliver.

"At TI, we invite you to experience the difference between compromise and choice — the difference between an ASIC device and an ASIC solution."

Wally Rhines

Walden C. Rhines, Ph.D.
Executive Vice President, Semiconductor Group
Texas Instruments Incorporated

At TI, we cover your ASIC needs from silicon to software to service and support.

Few ASIC suppliers match TI's breadth of choice and depth of support in helping you develop the most efficient round peg for a round hole. As you see below, our ASIC family spans the architectural spectrum from PLDs to standard cells.

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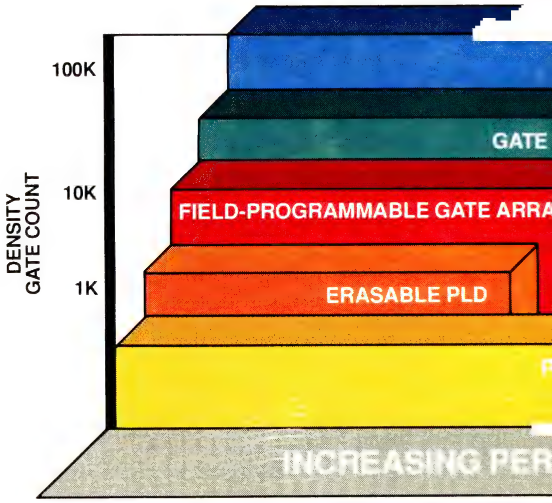
PLDs are a low-risk, affordable design solution for high-speed-logic consolidation. Stocked on TI distributors' shelves, they allow a quick ramp to volume production.

TI offers more than 40 PLD functions in industry-standard architectures, including the high-speed, 7.5-ns TIBPAL16XX-7 and TIBPAL20XX-7. For high-performance applications, TI also offers unique functions such as the programmable sequence generator, TIBPSG507, and one of industry's fastest programmable address decoders, the 6-ns TIBPAL18N8-6.

TI's ASIC PRODUC



Programming is quick and easy using readily available, third-party design software and programming hardware. For your high-volume production requirements, programming and testing services are available both from TI and authorized distributors.

When low power and reprogrammability are important, an erasable PLD (EPLD) gives you the freedom to make design changes quickly and easily. For high-volume production requirements, EPLDs are also available in one-time-programmable plastic packages.

To move your EPLD design rapidly from concept to silicon, the TI EPLD Development System accepts a variety of entry formats. These include schematic capture, Boolean equations, state-machine diagrams, and truth tables. TI's desktop CAE tool runs on an IBM®-compatible PC-AT™.

FPGAs: Best of two worlds

Like PLDs, FPGAs are user programmable, provide rapid design and debug, are simple to use, and are virtually risk-free. Like masked gate arrays, FPGAs feature high gate densities, high performance, a large number of user-definable I/Os, and a gate array-like design environment.

Currently available are TI's TPC1010A (1200 gates) and the TPC1020A (2000), with higher densities to follow. Unlike PLDs and gate arrays, FPGAs have a unique architecture that allows 100% observability of the internal circuitry. This provides flexibility of design verification, either "in-circuit" or "in the programming box."

The TI Action Logic System (TI-ALS) is a powerful development tool for implementing your FPGA designs while avoiding NRE fees. The TI-ALS accepts designs from popular CAE software packages including Viewlogic™, OrCAD™, Mentor Graphics™, and Valid™ — resident on PC386, Apollo™, and Sun-3™ platforms.

Gate arrays for greater differentiation

For applications requiring higher-density, high-performance ASICs with fast prototype delivery, TI's TGC100 Series 1-micron gate arrays are an excellent choice. Offering gate-array complexities up to 26K gates and 256 I/Os, the TGC100 Series utilizes familiar general-purpose logic libraries. You can define macros and pinouts, as well as specify packages with pin counts up to 256 pins.

A comprehensive design kit provides the information you need to easily implement your gate-array design.

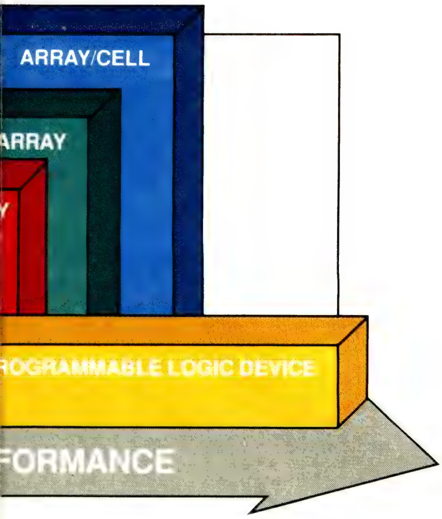
ASIC design centers, located at TI's Regional Technology Centers, are staffed with design specialists who are ready to help you.

Standard cells: As specific, as complex as you need

For ultimate performance and system integration, TI's TSC500 Series is your choice. The extensive cell library contains high-performance memory, register files, FIFOs, and MegaModule™ building blocks. Realizing the need to incorporate design-for-test into today's high-density ASICs, TI also includes JTAG-compatible SCOPE™ testability cells in its library.

Thus, you can tailor a standard-cell design to meet your exact system requirements. As with our gate arrays, a design kit is available, as well as technical design assistance through TI's ASIC design centers.

T SPECTRUM



> **"I need a high-speed part with unique functionality. Standard architecture is a big priority, too. Plus, I'm going into production and need volume delivery now."**

The TI Solution:

Programmable Logic Devices

For details about the support and service TI offers, please turn the page.

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

ASICs – Choice not compromise

IN THE ERA OF
MegaChip
TECHNOLOGIES

IN THE ERA OF MEGACHIP TECHNOLOGIES

On my schedule, ivery delays and necessary risks are t. Our design quires the density of ate array, but we ed to handle all the ogrammation rselves.”

e TI Solution:

ield-Programmable Gate Arrays

“The system my team is designing calls for a high-density, high-performance ASIC. I want to call the shots on pin count, pinout definition, and the package itself. Fast prototype cycle time, JIT delivery, and low cost are mandatory.”

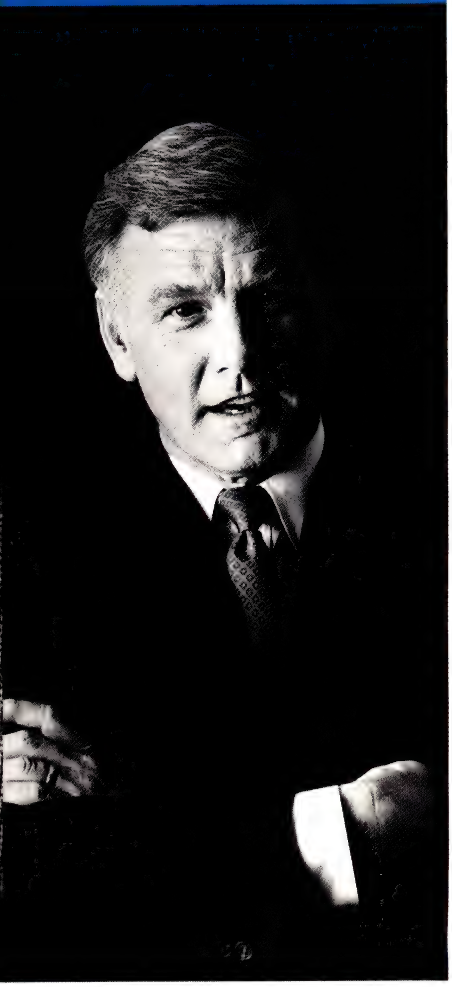
The TI Solution:

Gate Arrays

“We are developing a unique product that requires high-speed memory and other complex functions integrated on the same chip. Surface-mount, high-pin-count packaging is a major requirement.”

The TI Solution:

Standard Cells



A PERSPECTIVE ON ASIC DESIGN

The sun never sets on TI's service and support.

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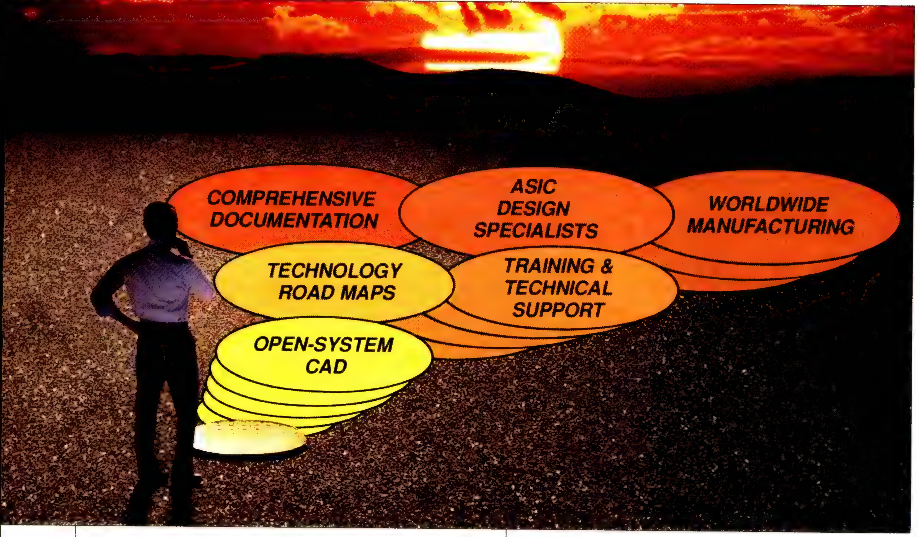
Our design flow is straightforward and minimizes the possibility of surprises.



Our worldwide wafer-fabrication capability is unmatched and moving into the submicron era. We have disclosed a 106K gate array fabricated with our EPIC™-II, 0.8-micron BiCMOS process technology.

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Tailoring the "fit"

In these special instances, we will tailor our procedures to your needs, striving to be as "application specific" as the term implies.

For example, certain business issues become very important when a programmable ASIC is best for you. Here, rapidly changing market conditions require absolute supplier dependability.

We can work with you to maintain your inventory levels. We can adapt our production to support your ship-to-stock or just-in-time programs. And if you'd like, we can deliver programmed or unprogrammed PLDs and other ASICs symbolized to your specifications to reduce your internal handling.

We are well aware that an ASIC solution is more than silicon, more than standard service and support.

You may want us to analyze your evolving ASIC designs and needs with you in relation to our evolving technologies. We can "tweak" our design flow to suit your requirements and integrate our design tools within your proprietary CAD systems when required. If your design calls for a proprietary function, we can also create a custom cell to suit your needs.

TI's MegaChip™ Technologies are the means by which we can help you and your company get to market faster with better, more competitive products. Our emphasis on volume manufacturing of high-density circuits is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers.

We at TI are willing to go the extra mile in service and support in order to achieve the ASIC solution best for you.

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—Fred Molinari, President

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DT1492-F	16SE	12	1, 2, 4, 8	150	2	130/DAC	16	3075
DT1492-F	8DI	12	1, 2, 4, 8	150	2	130/DAC	16	3075
DT1492-G	16SE	12	1, 2, 4, 8	250	2	130/DAC	16	3515
DT1492-G	8DI	12	1, 2, 4, 8	250	2	130/DAC	16	3515
DT1492-L	4DI	12	1	750	2	130/DAC	16	4175
DT1495	16SE/8DI	12	1, 10, 100, 500	40/2.5	2	130/DAC	16	2525
DT1497	4DI	16	1	100	2	130/DAC	16	3515
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Circle 210

A REVAMPED WESCON MAKES ITS STAND

SAN FRANCISCO

It's round 2 of the conflict between Wescon and Comdex/Fall. For the second year in a row, two of the biggest electronics shows in the country will be going on at the same time, but this time the managers of Wescon are countering the threat by reorganizing their event.

The dates are Nov. 14 to 16 for Wescon in San Francisco—despite the Oct. 17 earthquake—and Nov. 13 to 17 for Comdex in Las Vegas. Comdex ranks as the premier personal computer show (see p. 93), and the Wescon people are taking advantage of that fact. They're touting the differences between their broad-based production and the more narrowly focused Comdex and similar shows [*Electronics,* November 1988, p. 87].

Wescon's organizers are offering an "executive day" geared to managers, which covers global marketing issues and U. S. competitiveness. They've recruited an industry iconoclast—T. J. Rodgers, president and chief executive officer of Cypress Semiconductor Corp.—as the show's keynote speaker. And for the first time they have grouped technical sessions into 12 technology tracks. These are organized with a theme for each day—components, excellence in manufacturing and engineering, and systems technology. An overview paper leads off each session.

"This way we can encourage people to come for a day or two for a concentrated dose of technology," says Dennis Leitterman, organizer of the technical program. "The overview paper is the glue that holds the session together, outlining the session and defining terms," says Leitterman, a network projects manager for Hewlett-Packard Co. in Cupertino, Calif.

In components, one track is routed through memories. The smart-memory session covers application-specific devices, which are proliferating in dozens of product categories and opening up a panoply of market niches.

The show's broad scope is one thing that sets Wescon apart from Comdex

Meanwhile, the ASIC/RISC technology track features a session on the next generation of reduced-instruction-set computing. Since so many makers of microprocessors have jumped on the RISC bandwagon, the debate is no longer between complex-instruction-set computers and RISC, but which RISC processor to choose and how to fit it into systems. RISC software gets a technical session of its own and a discussion that includes how operating systems and compilers must be tailored to capitalize on RISC hardware. The session also explores porting applications to various platforms for broader acceptance of RISC.

Given that the average programmer can write only about a dozen lines of code a day, improving software productivity is getting a lot of attention. Users and vendors of computer-aided software-engineering tools report on improvements and their experience in selecting, using, and extending CASE tool capabilities.

Another session is devoted to computer-integrated manufacturing in semiconductor production. Users and vendors will focus on the implementation, problems, and benefits of CIM systems. The latest systems and the addition of control using simulation/models will be discussed.

Video systems, the topic of a special Wescon session, are being revolutionized by developments in electronic imaging and high-definition TV. This session will deal with the emerging video-systems standards and the developments affecting video systems in imaging, entertainment, and communications.

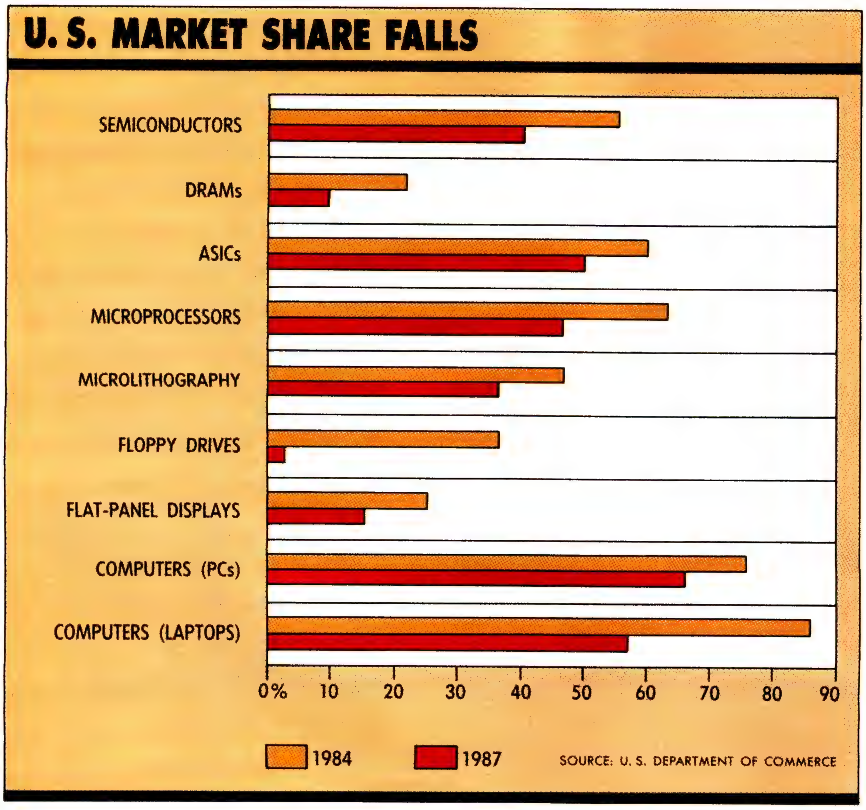
HOT TV. HDTV is one of the hottest issues in electronics, holding out the promise of revitalizing the U. S. industry. Acordingly, a two-hour presentation on the HDTV systems proposed to the Federal Communications Commission as a standard will be held each day of the show. The David Sarnoff Research Center, Philips Labs, and Zenith will make technical presentations on their HDTV schemes.

One industry segment that's rapidly settling on a standard is computer-aided design and engineering, which increasingly is turning to the Pentagon's VHSIC Hardware Description Language, or VHDL. A special session will report on VHDL design, synthesis, modeling, and testing.

Another growth area is in neural networks, which excel at tackling nonlinear dynamic problems. As a result, they are working their way into applications in robotics, signal processing, sonar, radar, fault diagnosis, and communications. One session examines what's involved in commercializing neural networks, and a special presentation looks at research and applications in Europe.

On a broader canvas, Wescon's executive day program takes up some global economic issues. One panel examines what the 1992 European Economic Community accords will mean for U. S. companies. Mario Belotti, an economist and professor at Santa Clara University, will deliver an economic forecast for 1990 and beyond.

And any discussion of world electronics markets usually includes discussion of a declining U. S. share. A key question for


U. S. MARKET SHARE FALLS

SOURCE: U. S. DEPARTMENT OF COMMERCE

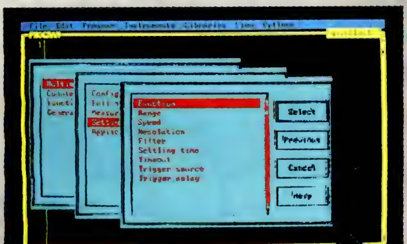
FLUKE AND PHILIPS – THE GLOBAL ALLIANCE IN TEST & MEASUREMENT

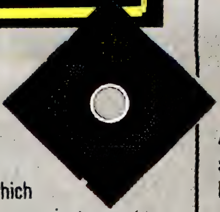
Motor control boards get the Alliance test

The alliance between test and measurement giants Fluke and Philips is excellent news if you're involved in configuring a GPIB test system controlled by a PC.

The two companies are among the world leaders in instrumentation for GPIB systems. Following the alliance between them the product range now offers the best choice for PC-based GPIB instrumentation systems including: oscilloscopes; generators; timer/counters; multimeters; switching and I/O; interfaces and software packages.

Software to cut development times





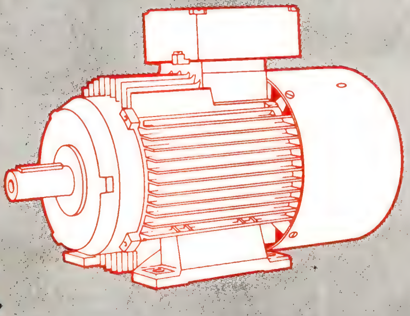
With Philips PM 2240 Test Team software your PC becomes a flexible GPIB instrument controller. Test Team contains a large library of instrument drivers which gives you complete control over your instruments without worrying about cryptic command strings.

With fast and simple program generation, plus ready-to-use graphics and analysis libraries, you can look forward to shorter development times.

GPIB interfaces for PC and PS/2

Philips offers GPIB interface cards for the PC (PM 2201) and for the PS/2 (PM 2202). All Philips GPIB software packages can be executed on PC and PS/2 and application programs written on PC can be executed on PS/2 and vice versa - that's part of our commitment to protect your investment now and in the future.

Motor Control PCB Tester



A company in The Netherlands has built a GPIB system for testing motor control printed circuit boards. The boards are built into a VME rack system used to control the heavy electrical motors in trams and trains.

This application uses two Fluke 8840 multimeters for various measurements on the PCBs. In this case the speed of data transmission over the system bus was the main reason for choosing the Fluke 8840.

Spotlight on Multimeters

The range of multimeters now offered by Fluke and Philips is one of the most comprehensive from a single supplier.
Specifications range from complex instruments for highly accurate bench measurements to tough go-anywhere handheld models for field work.
For systems builders, many models have the option of GPIB/IEEE 488, RS232 or other standard interfaces. This is encouraging for the builders of ATE since nearly every test system requires at least one multimeter and the Alliance now has a range to cover most applications.

For more information about PC controlled GPIB systems contact your local Philips sales office:

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For countries not listed, write to: Philips I&E, T&M Department, Building HKF, 5600 MD Eindhoven, The Netherlands.

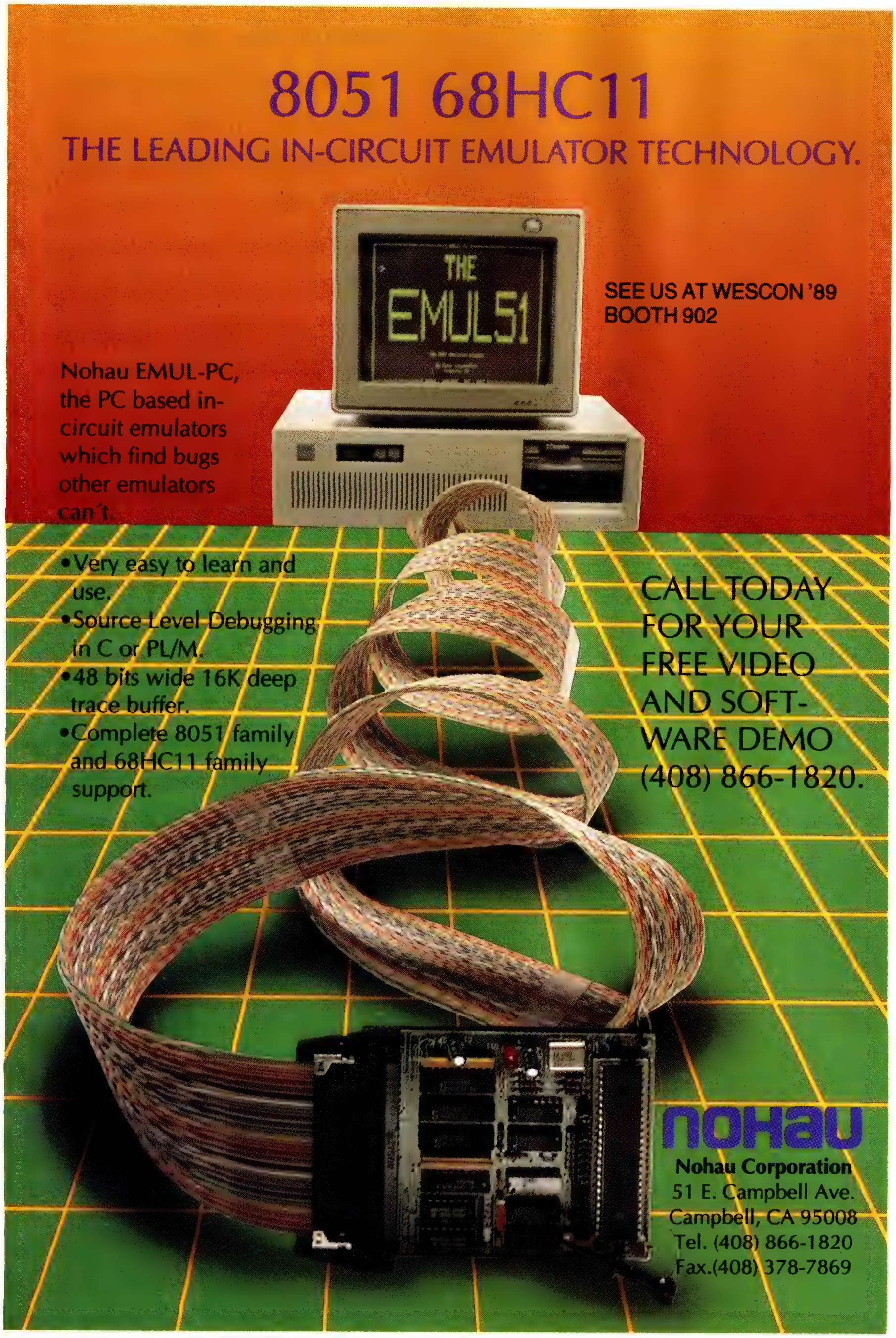
U. S. managers is how to strengthen American competitiveness. These issues are the subject of the keynote address. "If I had to draw a picture of what are the problems with American competitiveness, I'd blame one-sixth of this on Japanese companies, one-sixth on the U. S. labor force, and two-thirds on American management," says Cypress's Rodgers. "It's our problem and we've got to fix it, company by company."

Rodgers has become a vocal opponent of the formation of consortia, the granting of federal loan guarantees, and the revision of antitrust laws to allow consortia. "I don't think anybody in his right mind believes that the government should fix management problems by throwing money at them," he says.

The semiconductor business is a tough one, Rodgers says. Still, "I think Intel is a better-managed company than General Motors or U. S. Steel." The U. S. manages development better than its Japanese counterparts, he says, but American manufacturing management needs to be improved and the issue of quality control must be addressed.

The jolt for the chip business, he says, was a Hewlett-Packard study of semiconductor quality in the late 1970s in Japan and the U. S. American companies were "appallingly worse," Rodgers says. As a result, "every semiconductor company I know of put on the afterburners and tried to bring quality back. We've already come a long way, but we're not equal to Japan yet."

In terms of improving management skills, Rodgers points out that U. S. companies, unlike those in Japan, typically are managed top-down, with little input from production workers. He notes that he sits in on such weekly meetings at the San Jose, Calif.-based Cypress. But he doesn't believe radical changes will help. "One of the solutions is to 'bravely do nothing.' Our system reacts and prepares itself if we just leave it alone and don't screw it up." *–Sherrie Van Tyle*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Circle 420

RISC BOARDS

BOARD MAKERS RIDE THE RISC BANDWAGON

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If the move to reduced-instruction-set microprocessors is a groundswell in the work-station market, it can be described as a stampede among manufacturers of single-board computers, accelerator boards, and array processors. At least six leading suppliers have taken the wraps off high-performance RISC-based add-in boards for personal computers and work stations this fall, with more developers sure to follow.

Board vendors are using RISC chips for the same reasons work-station builders are: to apply more processing power to a computing task than is possible with processors based on complex-instruction-set computing architectures. That power boost, along with the relatively low cost of add-in boards, appeals to users who hope to get more mileage out of their existing machines by sliding a new board into the chassis.

FIRST PAIRING. The latest and perhaps most ambitious of these efforts is the Skybolt, an application-accelerator board from Sky Computers Inc. of Chelmsford, Mass. Skybolt joins Intel Corp.'s i860 and i960 processors—the only pairing of these two chips available to date—to provide 40 million instructions per second of integer performance and 80 million floating-point operations per second of math power [*Electronics*, October 1989, p. 17]. Sky

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says such performance propels the board's VMEbus work-station host into the category of a desktop supercomputer suited for applications such as simulation, finite element analysis, and computational chemistry.

Intel's 64-bit i860 processor handles integer, floating-point, and graphics computations; the i960 is a 66-mips general-purpose RISC microprocessor. Sky employs the i960 for "housekeeping" functions, such as input/output, system diagnostics, and software booting. Of the half-dozen firms introducing RISC boards recently, five feature either the i860 or the i960; only one uses Motorola Inc.'s 88000 chip.

"The i860 is like a strip dragster," says Bruce Busch, president of Sky. "It goes real fast on the straightaway but doesn't do well on curves"—the housekeeping chores. "We assign those to the i960 and let the i860 scream along on high throughput," he says.

Busch says advanced C and Fortran compilers tailored to the i860 help speed applications. Sky embeds a vectorizing module in the compilers; the module automatically produces vectorized code during compilation. This approach is also used in supercomputer compilers to boost performance.

Two other vendors have announced i860-based boards. Mercury Computer Systems Inc. of Lowell, Mass., has an attached processor under development, the MC860 board, set for release in the first quarter of next year [*Electronics*, May 1989, p. 73]. Meanwhile, the SuperCard, an i860-based array processor from CSP Inc. of Billerica, Mass., is scheduled to ship next month.

The MC860 will bring 40-mips and 80-megaflops performance to Sun Microsystems Inc. or other VMEbus work stations running compute-intensive applications, including signal analysis, image processing, and econometric modeling.

A half-dozen vendors have taken the wraps off RISC add-in boards

Ed Marcato, product manager for the MC860, explains that Mercury's attached processor fills several roles. It can function as a subroutine engine—much as an array processor does—to accelerate a particular subroutine, such as a fast Fourier transform.

It can also operate as an accelerator board to run all or parts of a user's application faster than the host computer can. Or it can function as a typical attached processor, combining both of the other functions as well as offering users a rich environment for application development.

CSP chose the i860 chip for its SuperCard array-processor family because of its superior performance and ease of use, says David Leighty, vice president for marketing. "All you have to do is write an interface to block memory and you're off," he says.

NUMBER CRUNCHER. The SuperCard family excels at number-crunching tasks, such as FFTs. A 33-MHz i860 delivers 66 megaflops, enabling a user to perform a 1,024-point complex FFT in 0.96 ms. That compares with CSP's previous best time of 1.4 ms. Leighty says the board will appeal to users who are running applications in signal, seismic, and image processing on VMEbus, IBM Corp. PC AT bus, and Enhanced Industry Standard Architecture bus hosts.

Other recent RISC offerings include single-board computers from Force Computers Inc. of Campbell, Calif.; Heurikon Corp. of Madison, Wis.; and Tadpole Technology Inc. of Waltham, Mass. Of the three, only Force has opted to use the Motorola 88000 processor on its board. Both Heurikon and Tadpole are using the Intel i960 chip, although Tadpole also sells a single-board computer that it has built around the 88000 [*Electronics*, July 1989, p. 23].

Force is already delivering its three-

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board CPU-8X series. Based on a 20-MHz 88000 chip, it provides 34 mips per pair of boards. As many as 10 pairs can be grouped to deliver 340 mips per card cage in a single VMEbus backplane. Applications being targeted by Force include real-time computing and on-line transaction processing.

Heurikon and Tadpole were quick to latch onto the i960, announcing their boards simultaneously with Intel's official introduction of the processor. Heurikon will start delivering its 66-mips HK80/V960E board for real-time applications—such as communications, embedded control, and image processing—in the first quarter of next year.

Tadpole's TP960V will be available next month for use in similar applications. It uses either 20- or 33-MHz versions of the Intel chip to get 66 mips on a board. *–Lawrence Curran*

MICROCONTROLLERS

SIEMENS GETS SET WITH A HOMEMADE 16-BIT BOMBSHELL

MUNICH

Already a top producer of microcontrollers based on Intel Corp.'s architecture, Siemens AG is now poised to do battle using controllers based on its own design. And the first member of the West German company's new family is a real doozy: a 16-bit CMOS device that offers performance similar to that of reduced-instruction-set-computing chips and is up to 20 times more powerful than competitive 16-bit controllers.

The 80C166 owes its performance to a high level of integration and a design that marries the best features of a microprocessor to those of a microcontroller. The part is designed to meet the high-performance, time-critical requirements of real-time embedded-control applications.

The RISC-like device marries a microprocessor to a controller

Siemens's new device sports a 100-ns machine-cycle time at 20 MHz, with most instructions executed in one cycle—unparalleled performance for a single-chip microcontroller, according to the company. Up to now, such performance has been achieved only in digital signal and RISC processors, says Peter Bauer, marketing manager for microcomputer components at Siemens's Semiconductor Division in Munich.

The controller's interrupt response time is impressive: under worst-case conditions, it checks in at 400 ns when instructions are fetched from internal read-only memory. This figure compares with 1-to-5-μs interrupts for competitive devices, Bauer says. The device also features a four-stage pipeline architecture, which is common in RISC processors but not in microcontrollers. On top of all this comes the large memory space—16 Mbytes in future versions and 256 Kbytes in the first family member, which is scheduled to be released in sample quantities early next year.

A prime design feature distinguishing the 80C166 from other controllers is its integration of three independent systems: a high-performance microprocessor, a programmable interrupt system, and independent intelligent peripherals. Each system is designed so that a large number of real-time events can be processed while the device also provides computational power. This design allows for the incorporation of new embedded-control functions, an impossibility with current controllers, according to Siemens.

The modular peripheral system can be expanded to provide greater functionality, or it can be made smaller to reduce cost. "This [flexibility], implemented at the initial design, will allow Siemens to quickly make available a family of parts to effectively meet specific embedded-control market demands," says Rod G. Fleck, architecture project leader for microcomputer components.

The new design is yielding superior benchmark test results. Depending on application, the 80C166 has been rated 10 to 20 times more powerful than Intel's 80C196 and twice as powerful as Motorola Inc.'s 68020 microprocessor, according to Siemens. Bauer sees Motorola's 32-bit 68332 as coming closest in power to the Siemens 80C166.

Siemens has made a big commitment to move into the forefront in the 16-bit world and join the exclusive club of U. S. chip makers that have until now set the standards in microcontrollers and processors. Since 1986, the company has invested about 100 person-years in developing the hardware and software for the 80C166. That makes the microcontroller project the biggest that Siemens's Semiconductor Division has ever carried out in logic-device development.

Among the embedded-control applications being targeted by Siemens is the automotive sector, which has long been a driving force in microcontroller develop-

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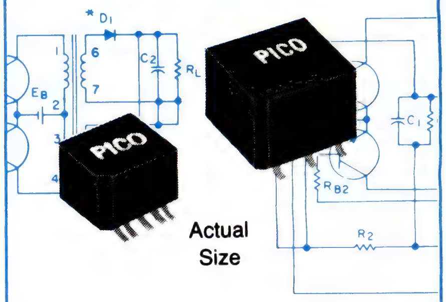

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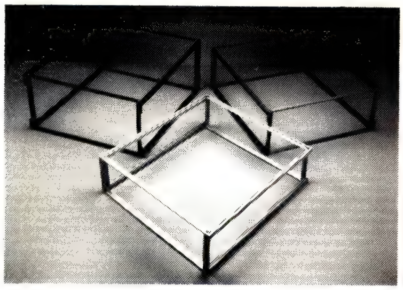

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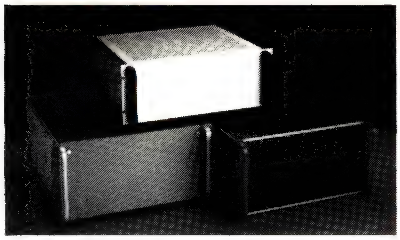

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ment. In this field, controllers must meet stringent demands under real-time conditions, such as in engine-management applications. Other uses are in the industrial field—robot control, process-automation systems with distributed intelligence, and control of asynchronous, servo, and stepping motors. In this area, Bauer says, are a large number of applications that could thus far be realized only with "classical" processor systems—those built with discrete subsystems such as a processor, interrupt controller, clock generator, and peripherals. But these systems have now reached the limits of cost and size to suit complex control applications.

Thanks to its high level of integration and more powerful architecture, the 80C166 can meet the time-critical demands encountered in such applications. It also suits the demands of data communications in such equipment as hard-disk drives. Small systems like these call for densely packed controllers boasting high performance and computing power.

Key to the 80C166's clout is its marriage of processor and controller functions. The device offers a state-of-the-art processor's large address space, flexible addressing modes, high computational speed, and easy programmability. It merges with a microcontroller's task-oriented architecture and fast interrupt response times, as well as a controller's ability to complete a task and context switch in one cycle and a widely configurable peripheral system.

In addition, the Siemens device has an internal direct-memory-address feature implemented with a peripheral event controller (PEC). By handling data transfers between the memory and peripherals in parallel with its central processing tasks, the PEC frees the CPU from having to perform primitive service tasks.

Other processor systems that sport a high level of integration typically incorporate the problems and bottlenecks inherent in such systems. For instance, all information tends to be routed over one bus, and interrupt response times are relatively sluggish. In such systems, peripherals must be made more intelligent and autonomous to pick up the slack. That means less flexibility, poorer scheduling and prioritization, and greater complexity and cost.

In the 80C166, the important operative elements for a task reside in the CPU. They are thus flexibly programmable for various applications and easy to prioritize. From a performance standpoint, the 80C166 CPU is comparable to a RISC processor in that it processes virtually all instructions in one cycle.

The 80C166 uses Siemens's 1.0-μm Acmos (for advanced CMOS) technology, derived from the process the company employs for fabricating 1-Mbit dynamic random-access memories. Contained in a 100-pin plastic quad flat pack, the device will be ready as samples during the first quarter of next year and is slated for volume production in 1991. Siemens will not disclose pricing plans, but Bauer says users will get more performance for the dollar compared with competing 16-bit microcontrollers. *–John Gosch*

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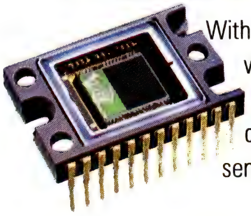

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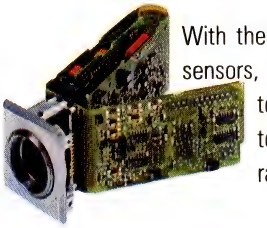

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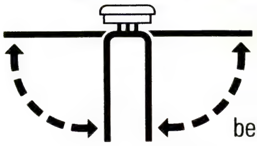

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HERE'S AN IC TO DECODE ALL TV SOUND NORMS

ITT Semiconductors' NIP2400, the world's first multistandard decoder IC for TV sound signals, crams 170,000 transistor functions on a 50 mm^2 chip that processes any TV sound signal.

FREIBURG, WEST GERMANY

The need to deal with different sound standards in different countries has been a perpetual headache for Europe's producers of TV sets. But the pain may soon be a memory now that the ITT Semiconductors Group is coming out with a chip that can handle any norm in use across the Continent.

The device, the world's first multistandard decoder IC for TV sound signals, also helps cut the audio-processing circuitry in a digital receiver to just three chips, a triumph in high-level integration.

The current standards scenario in Europe is a hodgepodge. While France has amplitude-modulated audio, most other countries use frequency modulation. In addition to FM, West Germany and the Benelux countries have analog stereo sound, whereas Scandinavian nations have adopted the digital Nicam standard for terrestrial stereo transmissions. Nicam, which stands for Near Instantaneous Companding System, is an invention of the British Broadcasting Corp.

To make matters more complex, the UK is considering a Nicam version different from that used in Scandinavia. As for satellite transmissions, France and West Germany use the digital D2-MAC audio standard, which other countries are likely to adopt as well.

The result is that TV receivers exported to different countries must be adapted to the prevailing sound standard. And viewers in border areas cannot receive programs from neighboring countries unless their sets contain the appropriate decoder and demodulator circuitry.

Enter ITT Semiconductors' all-norm demodulator-decoder chip, the NIP2400. Developed at the group's Intermetall GmbH subsidiary in Freiburg, the chip underlines a product strategy the company has followed with its devices for picture and text processing: design circuits that can handle any existing video and text standard for best advantage to set makers and users.

PRICE CEILING. The industry won't have to wait long to reap the benefits of the NIP2400. Engineering samples are now available and volume production should start early next year. The chip, made in 1.5-μm CMOS technology, is expected to cost less than $10 apiece in volume quantities, a beneficiary of Intermetall's policy of a $10 price ceiling for any consumer-type circuit it sells.

For that money, set makers will get a star performer, a circuit that integrates some 170,000 transistor functions on a 50-mm^2 chip and processes any sound-signal standard. Of note, too, is its high replacement value. For example, in Nicam decoding—it can handle both the British and Scandinavian versions—the chip replaces a conventional Nicam printed-circuit board containing three ICs and two to three quartz crystals, says Thomas Hilpert, developer of the 2400 in Intermetall's Concept Engineering department.

The circuit is designed to operate in partly or fully digitized TV sets using, for example, the ITT Digit 2000 chip set. It performs digital demodulation and decoding of Nicam-coded TV stereo sound as well as demodulation of FM and AM mono sound. What's more, it processes FM stereo TV sound according to the German/Benelux stereo transmissions norms. "So, given its flexible application, the IC is a practical solution to set makers' standards problems in Europe," Hilpert says.

In doing its job, the 2400 handles all demodulation and filtering right on-chip and programs these processes individually. It descrambles the signals as is required in a pay-TV application. The chip needs only one clock and works without any external filter hardware.

The IC's inputs are analog audio signals coming from the sound intermediate-frequency stage. These signals are digitized on-chip. They may contain audio information at a frequency from 4 to 7 MHz, corresponding to the individual standards. An external 18.432-MHz quartz supplies the pulses to an on-chip variable, digitally controlled oscillator that generates the clock for the 2400 and for subsequent audio stages. The chip outputs are up to three different audio baseband channels.

ANY STANDARD. By way of programmable parameters for the quadrature mixers and filters, the 2400 can be adapted to any European audio standard. Parameter programming, Hilpert explains, is by means of signals coming from the Digit 2000's microprocessor-based central control unit and fed to the 2400 via the IM-bus, an Intermetall bus.

For complete sound processing, the NIP2400 works with two other audio circuits: the audio mixing unit AMU2481 and the audio control processor ACP2371. The AMU controls the sound sources. Also, since the FM and AM channels coming from the 2400 have a sampling frequency of 64 KHz, the AMU converts the sampling signal to the Nicam audio sample rate of 32 KHz. It also handles deemphasis and dematrixing functions.

The ACP basically decodes the signal identification, keeps tabs on digital baseband processing functions such as volume, bass, and treble, and finally converts the sound channels to analog signals. *–John Gosch*

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LASERS

A SURPRISE WINNER IN SLAB LASER RACE

MUNICH

The global race to market a new type of laser has apparently been won by a small West German startup. The device, called a slab laser, is a solid-state laser excited by a flash or arc lamp; it provides more output power, better beam quality, and greater stability than conventional solid-state lasers.

Although a number of European companies and research institutes are cooperating in developing slab lasers in a pan-European project called Eurolaser, Munich Laser Systems GmbH has come from behind to build a prototype in just 14 months. It is now offering a perfected system, by the firm's own account the world's first slab laser to go commercial. And the 50-person, $5 million company, located in Munich's sprawling Technology Center, did its development without any funding from European or West German government authorities, says Leo Ploner, marketing director.

Munich Laser Systems is a spinoff from the West German subsidiary of laser specialist Coherent Inc. of Palo Alto, Calif. The company, founded in 1985 by seven engineers formerly with Coherent, has been growing by leaps and bounds. Sales have doubled from year to year, and they are expected to top $7.5 million this year. With the recent establishment of Munich Laser Systems Inc. in Montville, N. J., the company has made a firm commitment to sell and support its products in the U. S. Its prime business is in laser trimming equipment.

The slab laser gets its name from the geometry of its crystal, the active material in the device. Instead of the rod shape used in conventional solid-state lasers, the slab laser's crystal is a rectangular plate. It features slanted end faces that cause the infrared beam within the crystal to travel in a zigzag path. With this longer route, the output is higher than that of a rod laser, whose beam follows a straight line.

The slab laser was invented more than 10 years ago by engineers at General Electric Co. in the U. S. It became the subject of worldwide development efforts, but its commercialization has been delayed by a number of problems, including finding a good cooling system.

The slab laser's output power is about twice that of a single-cavity rod laser

Coming up with an efficient cooling system was in fact the toughest problem Munich Laser Systems faced in developing its product. The company is reluctant to give details on how it solved the problem for competitive reasons.

Ploner does say, however, that extensive computer simulations were necessary to determine the precise heat distribution within the crystal. In the effort to find a means for cooling the crystal surface to prevent internal heat pockets from producing cracks in the material, "we broke innumerable crystals," he says. "But in a long trial-and-error process with a number of designs, we finally solved the cooling problem."

The Munich laser's crystal is about 20 cm long and is made of neodymium-doped yttrium aluminum garnet. Its output power is 750 W, about twice that of a single-cavity rod laser, Ploner says. He expects the output eventually to reach 1,000 W. A higher output means that the laser can cut, drill, or weld materials much faster than a lower-power laser.

Another big plus for the slab laser is its high beam quality. In rod lasers, the temperature distribution causes undesirable bifocusing and depolarization. The slab crystal does not produce these effects; when the slab laser's beam moves down the crystal on its zigzag course, any optical disturbances cancel each other. That translates into a beam divergence that is small and constant over the laser's entire power range.

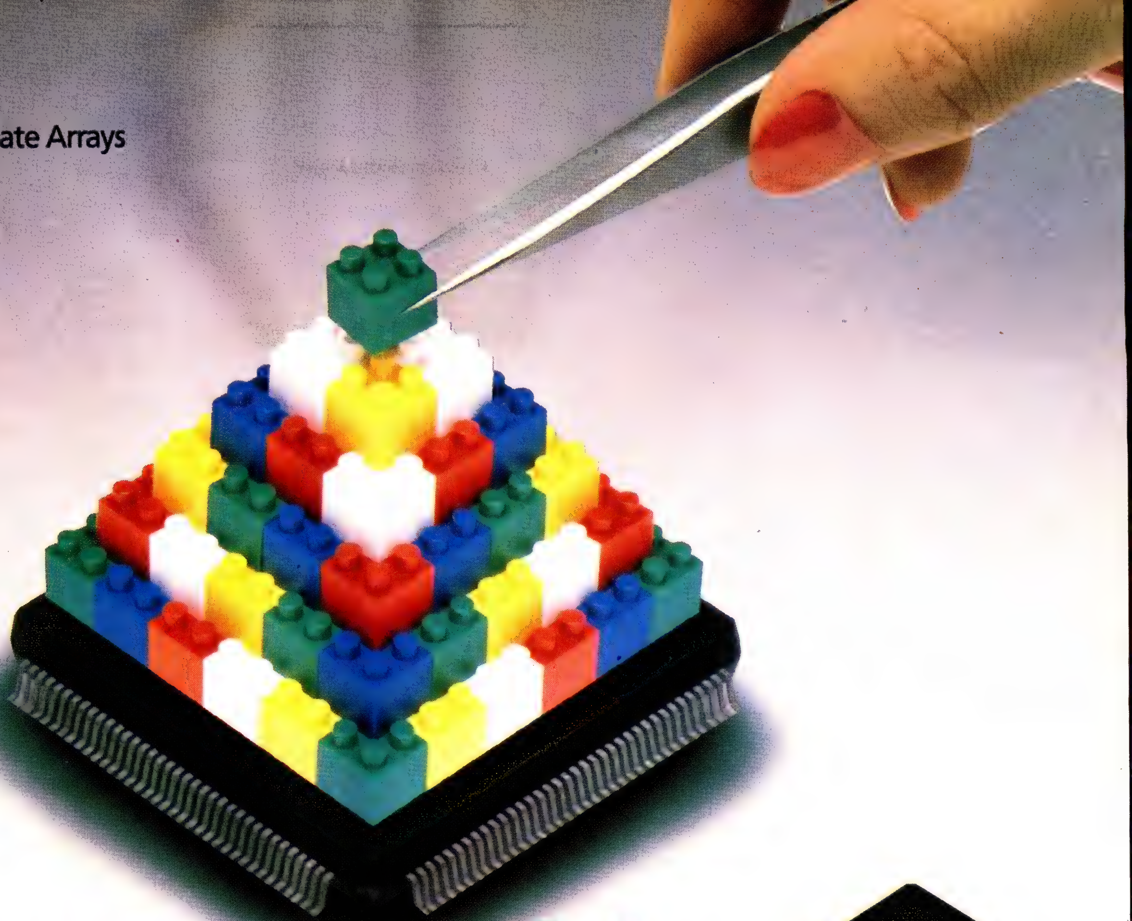
Because the divergence is constant, the beam can be coupled into an optical fiber without problems. For beam guidance, no complex and loss-prone mirror deflection systems are needed. Given the flexibility of fiber, the energy from the slab laser can easily be directed to where it is needed, even under awkward and confined space conditions.

Because of its short wavelength, a slab laser is generally better suited for material processing than the carbon-dioxide type normally used for the job. At 1.06 μm, its wavelength is 10 times shorter than that of a CO_2 laser. For that reason, most materials absorb energy at a rate three times higher. The high absorption makes the slab laser an ideal tool for processing materials such as copper, aluminum, gold, and ceramics—materials a CO_2 laser cannot readily handle.

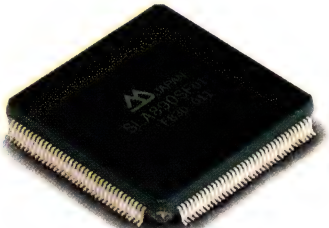
The slab laser's higher absorption also offers advantages in processing steel, Ploner points out. Since the material absorbs a bigger part of the light energy directly, the zone subjected to heat in, say, a welding process is smaller. That reduces stress and the likelihood of cracks

Munich Laser Systems has outgunned the pan-European Eurolaser project to make the first commercial slab laser (housed in the casing at left).

SLA8000 Series
CMOS High Speed Gate Arrays



System on Chip



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Gates (2-input-NAND)		5.304	9.416	14.336	18.300	22.680	30.000	38.550
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I/O Level		TTL, CMOS						
Delay Time	*Internal Gates*	0,47 ns typ.						
	Input Buffer	1,4 ns typ.						
	Output Buffer	3,5 ns typ. CL 15 pF						
Total I/O Pads		82	108	136	152	168	194	222
Total Power/GND Pads		4	4	4	4	4	4	4
Output Mode		Normal, Open-drain, 3-state, Bi-directional						

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Circle 100

in the material. By contrast, in welding with the longer-wavelength CO_2 laser, much of the energy is coupled into the material via the plasma cloud that the heat produces through evaporation, making for a bigger heat-subjected zone. Further, the plasma cloud results in undesirable "nailhead" seams—so-called because they are relatively broad on top. The slab laser produces uniformly narrow and clean welding seams.

Still another advantage is that the slab laser provides a simple beam-guidance system. A CO_2 laser's beam can be guided only by deflection mirrors. But in many applications, such as robotized laser equipment working along several axes, mirror deflection can be complicated and energy-consuming. Some robots with an integrated CO_2 laser use more than 10 mirrors, with each one accounting for an energy loss of 2%. What's more, the mirrors require cleaning and frequent adjustments, and that slows down the material-processing job.

With the slab laser, however, beam guidance and energy delivery are simple and result in no energy loss. The optical fiber into which the energy can easily be coupled brings the energy without loss to the spot where it is wanted. Also, there are no mirrors to adjust and clean, which minimizes maintenance. *–John Gosch*

PERSONAL COMPUTERS

TANDY BUYS INTO EUROPE'S PC MARKET

MILAN

A new alliance in Europe's middle-level personal computer market promises to intensify the battle to sell low-priced, high-performance machines. The decision of U. S.-based Tandy Corp. last month to acquire PC maker Victor Technologies of Stockholm pits that duo against two other combatants: U. S.-based Tandon Corp. and France's Bull SA, which recently acquired Zenith Electronics Corp.'s computer business.

The three contestants are vying for share in a booming European PC market. Most analysts predict 30% to 35% growth in this segment next year. Tandon recorded $459.8 million in sales last year for 3.8% of the market, according to Dataquest Intelligent Electronics in Paris. Victor posted $406.5 million in sales for 3%, while Zenith accounted for $394 million in sales and a 2.7% market share.

What makes Victor Technologies—which sells a standard line of PCs and hand-held computers built with technology licensed from Japan's Kyocera Corp.—especially appealing to Tandy is its excellent third-party distribution system in England and on the Continent. Tandy has not had much success with its retail stores in Europe.

"The company never got to the business market," says Gordon Curran, a director of Dataquest Intelligent Electronics. That failure has prevented the Fort Worth, Texas, computer maker from developing volume European PC sales overall. "Perhaps it sells 35,000 units in a European market of 4.6 million units," says Curran. "Victor already sells more than 100,000 units."

The key for Tandy is to retain Victor's third-party distributors. "Distribution is the key to this business," notes Curran. "If Tandy can keep Victor's network, it will have a real advantage."

Tandy and Victor have very similar marketing strategies: both compete on price. Although Tandy won't say which of its products it will sell through Victor, it is expected to use the Victor brand name and distribution system as an outlet for its own products. The mix should enable Tandy to adjust prices better. "The two product lines can be expected to merge here in Europe," says Curran.

This strategy is particularly important in the middle-level PC market, which continues to be squeezed by lower profit margins. "Keeping up a high volume of sales is crucial to survival in these low-profit days," says Nizam Hamid, an electronics analyst with UBS-Philips and Drew in London. "Since the European market will continue to grow faster than the U. S. market, access to the market here can only do a company good."

Because Victor assembles its computers within the European Community, the $120 million acquisition means Tandy will not be shut out of the unified European market. As the EC elaborates its "local content" rules, it is expected to require manufacturers to buy 68% of their computers' parts from within the 12 EC nations. "Acquisition is the royal road into the Single Internal Market," says Hamid. "Tandy's move is a remarkably low-cost way to get in."

Tandy says it plans to use the European manufacturing base to produce OEM products for the European market. "We have long-term agreements with Digital [Equipment Corp.] and Matsushita to produce a line of personal computers in their name," a Tandy spokesman says. "We can use our European plants to continue this relationship."

Victor is currently owned by Datatronics AB of Stockholm, which was founded by the Scandinavian information technology pioneer Matt Gabrielson. Garielson is credited with having a "visionary" understanding of the Scandinavian computer market, and he is expected to continue on the board of the company after the purchase. His presence should help Victor conserve its Northern European market share. *–Andrew Rosenbaum*

ISDN

NYNEX FINDS A UNIQUE DEVELOPMENT PARTNER

LONDON

Nynex Corp. has found an intriguing proving ground for testing some new telecommunications technology: the British crown colony of Gibraltar.

The New York-based Bell regional holding company is upgrading Gibraltar's phone system to accommodate a broadband integrated services digital network. The ISDN system will be installed and operated by a new company to be formed as a joint venture by Nynex and the Gibraltar government.

The network will be based on an optical-fiber backbone transmission system. Data traffic and TV signals will be switched through the network and delivered to residential and business subscribers via coaxial cable.

For Nynex, which runs telephone services in New York state and New England, the project is its first involvement in running an overseas public phone company. Nynex will commit $10 million to the venture, says Irvine Nazzario, director of international operations. He adds that the new Gibraltar network will be the first public telephone system designed to switch wideband video and telephone traffic over the same cables.

Nynex is the only one of the seven Bell regional holding companies to run its own research and development laboratories. It has some 300 to 400 staffers working on various telecom technology projects, including wireless local-area networks, artificial-intelligence applications, network management schemes, and broadband switching and transmission systems. The colony of Gibraltar will provide a testing ground for some of this work, Nazzario says. "We expect to install some systems that we are experimenting with in the U. S.," he says. *–Peter Fletcher*

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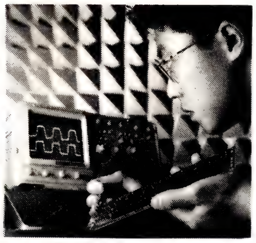
EMC MICROWAVE

Crossing the technical barrier with Murata's human technology. Vol.3.



Analyzing Effects of Noise Suppression in the Electromagnetic Anechoic Chamber.
Oscilloscope assessment of noise-suppression performance of the NFV610 mounted on a digital circuit.

A NEW "WAVE" IN NOISE SUPPRESSION — PERFECTING THE WAVE SHAPE

Continuious technological inovations for ever changing Market needs. — Murata.

The recent popularity of digital equipment has brought with it the serious problem of harmful noise and has created a demand for advanced EMI suppression technology. This noise-suppression technology has become indispensable, including the development of noise filters exhibiting superior characteristics.
Murata's EMI Suppression Division Manager, Mr. Sakamoto, discussed Murata's many years of experience in the field of digital noise suppression.

Q: When did Murata launch its noise suppression program?

A: About thirty years ago, Murata started production of electronic components for noise suppression, centered on telecommunications equipment. It was around 1979, however, when the company really went full stride into the problem. Murata looked to the future by developing its original three-terminal capacitor to meet stringent FCC noise regulations.

Q: Was R&D conducted in the electromagnetic anechoic chamber at Murata from the very beginning?

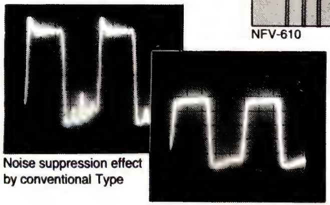
A: No. At first, all experiments were performed outdoors, with the facilities limited to a receiver and an antenna. It was a long series of tests by trial-and-error to search for the most effective filter for the intended purpose. The electromagnetic anechoic chamber which Murata introduced later is the consequence of pioneering in this field far ahead of others in the industry.

Q: Murata has a very fine reputation in noise suppression technology in digital equipment, doesn't it?

A: From the very beginning, Murata has concentrated on suppression of noise from within equipment. Moreover, it has been Murata's consistent policy to develop new products by listening to the problems raised by our customers. This mutual cooperation between maker and consumer has contributed much toward the accumulation of practical know-how on noise suppression.

Q: Is this know-how reflected in the recent NFV610 series?

A: Yes. When removing noise with filters available thus far on the market, the signal waveform tended to round excessively or else became distorted. With our new NFV610, the wave-shape function preserves the original waveform while eliminating noise effectively. Thus, this new product is ideal for application in signal lines.



Noise suppression effect by conventional Type

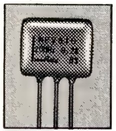
Noise suppression effect by NFV610

Q: We have heard that the new product is highly effective also for suppressing noise from digital displays. Could you elaborate on this?

A: Upon removal of noise, an RGB signal normally tends to round and its resolution drops. This particular problem, judged by many as difficult to solve, has now been solved by the new NFV610.

Q: What are other possible applications besides displays?

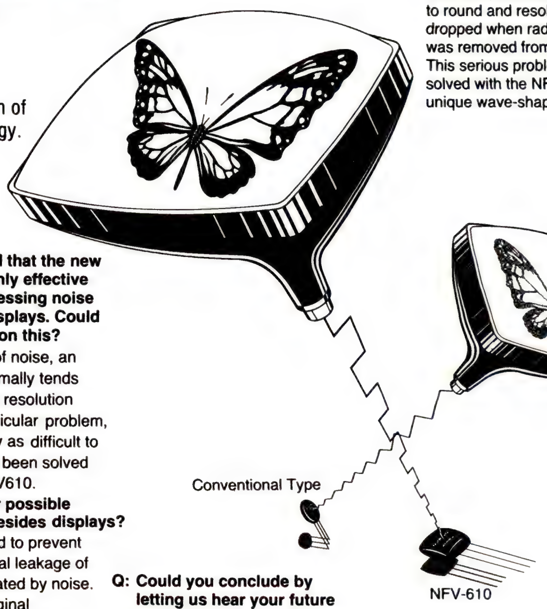
A: It can be applied to prevent the problematical leakage of information created by noise. In short, the original information (signal) can be reproduced by shaping the noise picked up; but this is prevented with the filter. Another application is in such equipment as HDTV and EDTV, where digital processing in higher frequencies is required.



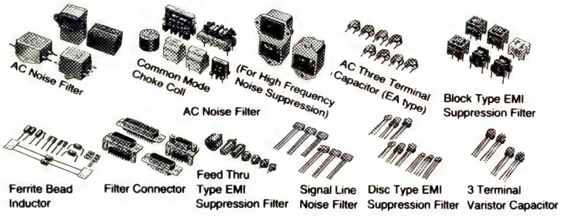
NFV-610

Q: Could you conclude by letting us hear your future aspirations?

A: In line with the company policy to continue consulting customers about all forms of noise-suppression measures, Murata is dedicated to the supply of its technology without reluctance. Simultaneously, Murata is pledged to solve each and every problem raised by consumers through mutual cooperation and to contribute toward the cleanliness of the electromagnetic environment.



Wave-Shape Function
Until now, waveforms tended to round and resolution dropped when radiation noise was removed from RGB signals. This serious problem is now solved with the NFV610 and its unique wave-shape function.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Circle 131

EUROPEAN OBSERVER

WILL THE TELECOM MERGER MANIA CONTINUE TO SPREAD?

Look for a new round of mergers, acquisitions, and joint ventures in the European Economic Community like the one between GEC Plessey Telecommunications Ltd. and Siemens AG, or AT&T Co. and Italtel of Italy. That's the prediction from market researchers at BIS Mackintosh Ltd. of Luton, England. Their forecast is contained in a study reporting that PABX markets in the EEC countries reached a value of $2.2 billion in 1988 and should hit $2.8 billion by 1992. The report points out that now the most vital factor affecting growth will be the introduction of mutual type-approval recognition (whereby equipment approved by certain labs will be approved for use in all countries), says Alan Pye, project director. Pye says that once a mutual-recognition policy has been put in place, manufacturers will be free to place more emphasis on their marketing policies. "The key to success in a reregulated market will then be distribution," he says, one of the main factors that will lead to mergers. ☐

WEST GERMANS PUT MORE CASH INTO JESSI

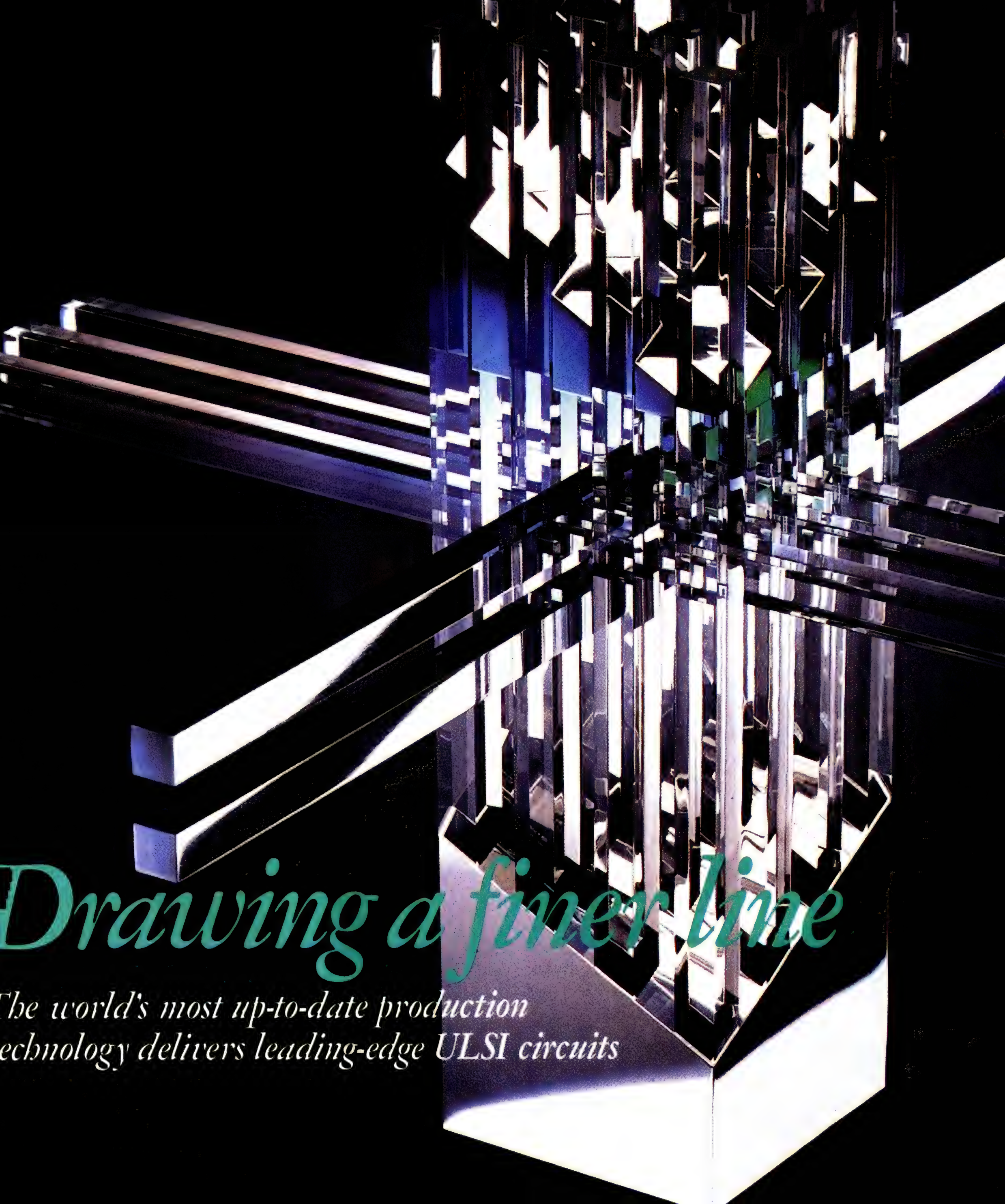
With the Joint European Submicron Silicon Initiative ready to start, West Germany's Ministry for Research and Technology is creating more research capacity. The idea is to ensure that the $4 billion, five-nation Jessi project achieves its goal of developing the tools and technologies needed to produce 64-Mbit DRAMs and similarly dense logic circuits by the mid-1990s. In the works is a $200 million research institute in Itzehoe, Germany, which is in the nation's northernmost state of Schleswig-Holstein, to be called the Institute for Silicon Technology. About two-thirds of the institute's activities will be in basic research and one-third in applications-oriented research: with these two efforts under one roof, government officials hope to avoid a gap between fundamental and applications-related research for the Jessi project. Also, with 90% of Europe's semiconductor production equipment coming from overseas, the ministry wants to boost activities in that sector. The five member nations of the Jessi consortium are France, the UK, Italy, the Netherlands, and West Germany. ☐

SLIDING DRAM PRICES SHOULD MEAN CHEAPER SRAMs

Plummeting prices for dynamic random-access memories mean equipment makers can look forward to lower prices for slow static RAMs next year. That's the reasoning of Dataquest Inc. analyst Byron Harding in London. A recent Dataquest study shows that Japanese chip manufacturers are slowing production of DRAMs as the current market glut brings prices down. "Given the oversupply of DRAMs, companies like Toshiba and Hitachi are looking to SRAMs, because their price remains relatively high," says Harding. "As SRAM production boosts, the chips should go down in price, to the benefit of manufacturers that make high-performance computers and work stations" employing cache memory, he says. ☐

MIPS, NIXDORF TO BLEND MUSCLE IN RISC TECHNOLOGY

An agreement between West Germany's Nixdorf Computer AG and MIPS Computer Systems Inc. of Sunnyvale, Calif., to cooperate in reduced-instruction-set-computer technology should considerably boost the popularity of the U. S. company's MIPS processors. The joint development activities are being undertaken to lead to processor architectures that will increase the power of Nixdorf's family of Targon computer systems. RISC technology, says Paderborn-based Nixdorf, will set the pace in the development of medium-sized computers of the 1990s and should shortly make it possible to attain performance of up to 100 million instructions/s. ☐



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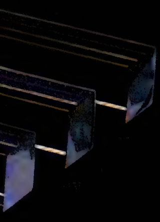

Sub-micron production in full swing, bringing the new age of 4M DRAMs

Oki's Miyagi Plant, benefitting from the latest advances in the company's system technology, has already reached mass production and shipment of 1M-bit memories and has recently begun quantity production of 4M DRAMs. At the Miyagi Plant, broad utilization of ultra-fine process technology and state-of-the-art automation combine to assure the high quality of these products. Oki is already well underway with technological innovation enabling production of 16M-bit memories.

High-level automation with ultra-fine process production

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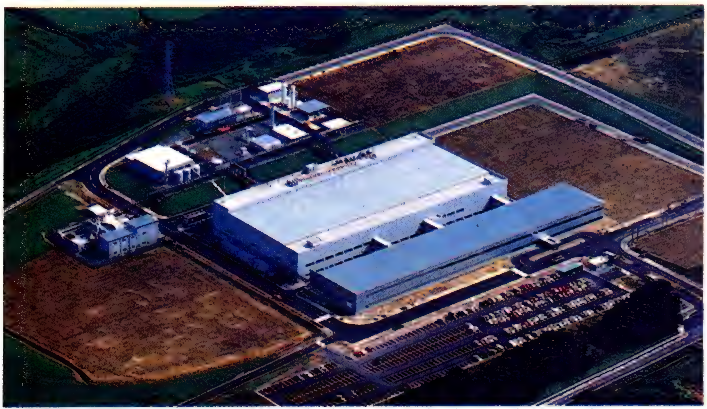

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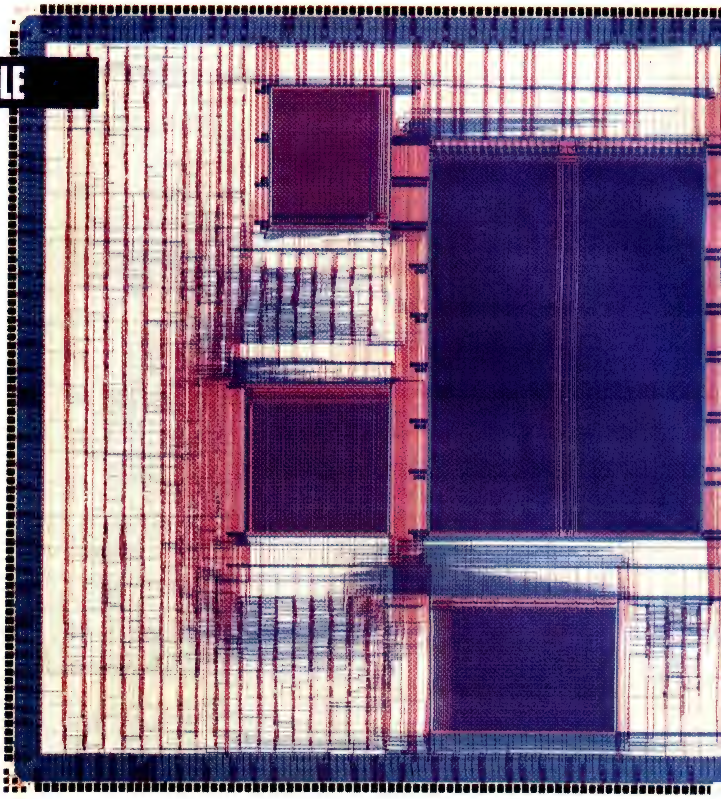
Oki Electric Industry Co., Ltd.
Tokyo, Japan

BY BERNARD C. COLE

MAKING THE RIGHT MOVES IN ASICs



LSI Logic combines the lower cost of gate arrays with the higher density of standard cells in its LEA100K family.

As the playing field shifts, ASIC vendors are retooling products and rethinking strategies

As application-specific integrated circuits become an ever bigger chunk of the semiconductor market, the competition among manufacturers is taking on the flavor of a global chess game. ASIC makers in the U. S., Japan, and Europe are mulling their moves as they navigate between two worlds.

On one side is the highly competitive gate-array arena, currently the biggest ASIC segment and one dominated by the Japanese. Here, parts are produced in high volumes at low profit margins. On the other side are standard-cell-based ASICs, lower-volume devices carrying higher price tags and higher margins. This segment, now the domain of the Americans, will take on more importance in the 1990s.

Tied to the shifting product mix is an ongoing revolution in process technology and software that has the playing field in a state of flux. The major international contenders are reassessing product and technology strategies, making strategic alliances, and looking into mergers and acquisitions. For the Japanese, the activity is aimed at moving more forcefully into cell-based ASICs, while the Europeans' goal is to get a better toehold on the market. The U. S. players, meanwhile, are looking to gain an edge through more sophisticated technology, especially mixed analog/digital designs.

At stake is participation in a market that by 1993 will rise to $12.5 billion and represent 21% of all IC sales, says market researcher Integrated Circuit Engineering Corp. The 1988 share was 15%, or $5.9 billion, according to the Scottsdale, Ariz., company's just-published report, *1990 ASIC Outlook*.

ICE says that gate arrays, which last year accounted for almost half of all ASICs sold, will diminish to about 42% of the total in 1993. Gaining market share at the high-density end of the spectrum are cell- and compiler-based circuits of 50,000 to 100,000 or more gates; this category will rise to 31% from 23% last year. Chipping away at the low end are programmable logic devices [*Electronics*, October 1989, p. 72]. As they move up in density to the 20,000-gate range, their share will rise to 13% in 1993 from 10% in 1988.

Also changing is where ASIC companies are making most of their money. In CMOS gate arrays, for example, half of all 1983 revenues were derived from nonrecurring engineering costs. This figure dipped to 33% in 1988 and will plummet to 20% by 1993, ICE says. The reasons for the change are increased competition among gate-array suppliers—there are now about 100 of them worldwide—and more sophisticated customers. ASIC users are taking on more and more of the design role, using the ASIC house as no more than a foundry.

Another wrinkle is a subtle shift in process technology. In both gate arrays and standard cells, growth is flattening in CMOS as biCMOS begins to gain ground. The next technology wave will undoubtedly be analog. By early next decade, more than half of all CMOS and biCMOS cell-based ASICs will have up to a quarter or more of their dice devoted to analog functions, predicts Boston's Technology Research Group Inc.

These changes are affecting Japanese manufacturers, who have considered gate arrays—particularly commodity CMOS circuits—their ASIC stronghold since the late 1970s. They supply 53% of these parts worldwide and U. S. vendors 36%, ICE says. Japanese presence in cell-based parts, by contrast, is a mere 25%, against almost 70% for the U. S.

But Japanese companies are not sitting still. With the help of commercial computer-aided-design development tools, they are looking to increase their penetration of the cell-based market as they simultaneously boost gate-array densities. Helping Japanese manufacturers in this effort are strategic alliances with other IC vendors and with CAD software houses.

For example, Hitachi Ltd. of Tokyo last year made a deal with VLSI Technology Inc.—No. 3 in cell-based ASIC sales worldwide—to exchange process expertise for the San Jose, Calif., company's proprietary software and CAD tools. Industry watchers expect Hitachi to become a major player in cell-based designs, especially with completion of fabrication facilities in the U. S.

Of all Japanese manufacturers, Toshiba Corp. has pursued the most balanced ASIC strategy, putting as much effort into standard cells as in gate arrays. Its fifth-place ranking in standard-cell ASICs comes through alliances, most notably an agreement with Siemens AG of West Germany and General Electric Co./RCA in the U. S. The partnership, called Advancell, creates an international standard-cell library for 1.5- and 1.0-μm processess that allows the three companies to second-source one another.

Toshiba has been working closely with CAD software vendors since 1987, first linking up with SDA Systems for its integrated design environment, then with Tangent Systems Inc. for its gate-array routing system (both companies are now part of Cadence Design Systems Inc. of San Jose). Last year the Tokyo company contracted with ViewLogic Systems Inc. of Marlboro, Mass., for its personal-computer-based design environment; most recently, it added support for the logic synthesis tools from Synopsys Inc. of Mountain View, Calif.

No. 2 in worldwide gate-array sales, NEC Corp. of Tokyo is looking to boost its No. 16 ranking in cell-based ASICs by means of CAD partnerships. The new breed of CAD tools from specialty software houses exceeds the capabilities of proprietary software, says Grant Hulse, strategic marketing director for NEC's ASIC Division in Mountain View. These tools can help ASIC houses deliver products faster by shifting more of the design function to the customer. Last summer the company made available to outside users its OpenCAD integrated tool set, which combines NEC's own arsenal of software with a variety of products from outside vendors. Included in the set are Synopsys for logic synthesis; HiLo, for system logic and timing simulations; and NEC's own floor planner for layout.

Like NEC, Fujitsu Ltd. is shifting to a more open CAD environment, says Ed Barnett, director of ASIC marketing for Fujitsu in San Jose. The Tokyo-based company—No. 1 in gate arrays and No. 20 in standard cells—in the middle of last year replaced its internally developed CAD system with a new solution. ViewCAD is an integrated work-station-based system offering complete design capability from schematic capture through simulation and verification with industry-standard CAD tools. Among these are Synopsys' logic-synthesis tools and the Verilog mixed-level simulator from Gateway Design Automation Corp. of Westford, Mass., now owned by Cadence. The system will be used in the 15 design centers Fujitsu is setting up in Europe and the seven being established in the U. S. The company is also building ASIC fabs in both areas.

PLAYING FOR MARKET SHARE

GATE ARRAYS
Total Market: $3.3 Billion
Japanese Share: 53%

	1989 Sales ($ Millions)
Fujitsu	535
NEC	530
LSI Logic	425
Toshiba	300
Hitachi	220
Motorola	180
National	148
Plessey	120

STANDARD CELLS
Total Market: $1.7 Billion
U.S. Share 65%-70%

	1989 Sales ($ Millions)
Texas Instruments	185
NCR	110
VLSI Technology	90
Oki	80
Toshiba	80
IMP	60
Mitsubishi	60
Harris	50

SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.

Europe, meanwhile, until relatively recently has taken a back seat to the U. S. and Japan. But a few companies are preventing a clean sweep of the European market—notably, the UK's Plessey Semiconductor, the French-Italian combine SGS-Thomson Microelectronics, and Siemens in West Germany. Philips International NV of the Netherlands, which already has second-sourcing deals with two U. S. suppliers, plans to debut its own biCMOS parts early next year.

The Philips biCMOS entry is a family of high-performance emitter-coupled-logic arrays with densities up to 180,000 gates, says Ata Khan, Philips' semicustom marketing manager in Santa Clara, Calif. Through its U. S. subsidiary, Signetics Corp. of Sunnyvale, Calif., Philips is also working with Texas Instruments Inc. of Dallas and VLSI Technology. Signetics expects to do about $20 million worth of business in gate arrays and $8 million in standard cells by second-sourcing TI's SystemCell family. It will also second-source VLSI Technology's 1.0-, 1.2, and 1.5-μm CMOS gate arrays.

The most established European player, Plessey, ranks eighth worldwide in gate-array sales. The Swindon company's muscle comes from its traditional market in bipolar TTL and ECL arrays. More recently, it gained analog strength by acquiring Ferranti Interdesign of Scotts Valley, Calif., a noted analog ASIC supplier, and digital clout by introducing new families of 1,000-to-110,000-gate CMOS devices. Plessey is now establishing itself in the standard-cell business with two CMOS families and one based on a proprietary current-mode-logic technology.

For its part, SGS-Thomson draws its strength from bipolar analog and mixed analog/digital arrays and from a digital line obtained through the acquisition of Mostek, from which it will see about $30 million in sales in 1989. The company has recently expanded its offerings with a digital CMOS gate-array family and a mixed-mode CMOS standard-cell series.

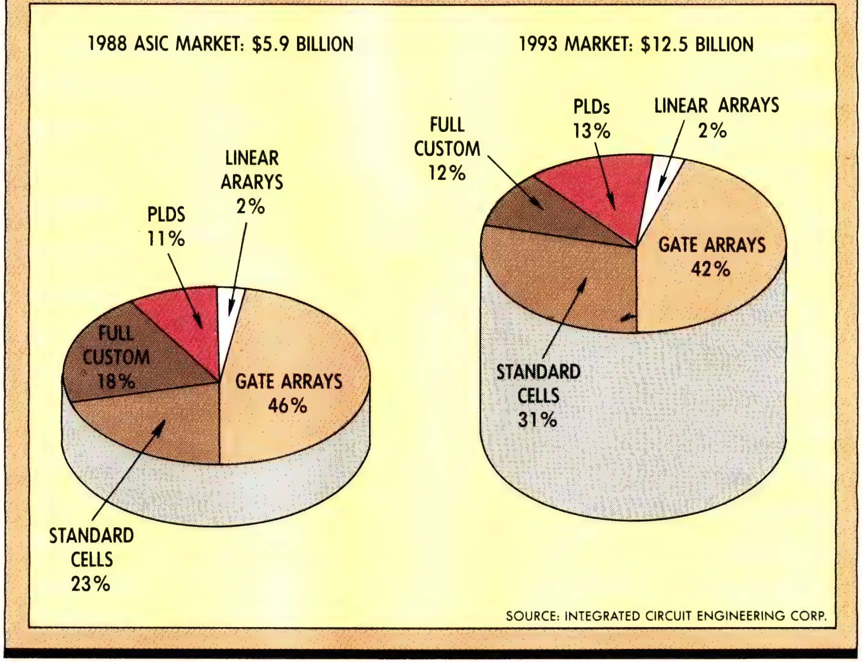
In the U. S., most ASIC efforts are in redirecting product development to high-performance, high-density niches in both gate arrays and standard cells, where there is less competition and higher margins. For example, to combine the lower cost and faster turnaround of gate arrays with the higher density of standard cells, LSI Logic Corp. last month introduced a new series of embedded arrays. The LEA100K family is made with the Milpitas, Calif., company's 0.7-μm CMOS channel-free, compacted-array technology.

Using LSI Logic's modular-design software with LEA100K, a designer can create an optimized cell-based ASIC of up to 150,000 gates, but with the last one or two layers unmodified. In this way, the user can build an inventory of wafers that can later be customized to specific system requirements by modification of the last layers. The customer retains the high-density advantage of standard cells but can reach prototype production in as little as 14 days, the same as for a gate array. "It is now possible to give the designer the benefits of both approaches while minimizing the disadvantages of each," says Brian Conners, vice president of strategic marketing at LSI Logic.

CAD software that is process-optimized plays a key role in exploiting the full potential of the LEA100K family, Conners says. To this end, LSI Logic is adding new tools to its Modular Design Environment, including the Design Builder and the Silicon Builder.

Developed to shorten the design cycle, Design Builder works with the company's Silicon Integrator package to aid designers in chip partitioning, die-size estimation, automatic memory-cell compilation, and synthesis of specialized logic functions.

STANDARD CELLS ON THE FAST TRACK



SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.

Gate arrays, now the single largest chunk of the ASIC market, are starting to lose ground to standard-cell-based devices on the high end and PLDs on the low.

Silicon Builder, meanwhile, works at the chip level to automatically produce physical block layouts of all the major design elements.

LSI Logic is giving in to customer pressure and adding a codesigner environment interface, which will allow linking to third-party software tools. Among the first outside tools to be added are Mentor Graphics Corp.'s Idea series design tools, the Synopsys logic synthesis software, and Crosscheck Technology Inc.'s testability and diagnostics software.

Motorola Inc. is also siding with the advocates of open architecture. The Phoenix, Ariz., company is gearing up for a major push in CMOS ASICs via its Open Architecture CAD System, which will allow systems designers to create high-density bipolar, CMOS, or biCMOS gate arrays and standard cells or a new type of ASIC that Motorola calls the customer-definable array, or CDA.

With the CDA approach, a user can combine the density of a standard cell and the turnaround time of a gate array, says Frank Reid, Motorola's bipolar array product manager. This is done by predefining the basic building blocks needed before actually designing the circuit. From this information, the system generates an application-specific set of gate-level cell-based tiles, a step that eliminates unnecessary gates. The result, says Reid, is a circuit that can be fabricated within existing gate-array channels using existing power and biasing grids with nearly 100% placement latitude.

Motorola uses the Electronic Data Interchange Format as the common backplane and combines a mixture of proprietary and commercially available tools. Among them are packages from Cadence, Gateway, Mentor Graphics, Synopsys, and Valid Logic, plus its own tools for static timing analysis and test-pattern generation.

Initially available on Open System will be Motorola's 1.0-μm three-layer-metal CMOS array with densities as high as 100,000 usable gates. According to Reid, the company expects to be up and running by January with a new family of 50,000-gate bipolar ECL arrays, followed by biCMOS devices later next year.

Also going toward a more open design environment is National Semiconductor Corp. The foundation of the Santa Clara company's Open Solutions program is a common backplane based on EDIF, says Robert Johnson, vice president of the ASIC Division. EDIF serves as the communications highway between process-specific data-automation software targeted at each of National's digital and mixed analog/digital, CMOS, and standard-cell ASIC efforts. Third-party software from a number of vendors can be easily tied in.

A preoccupation with CAD can also be seen at VLSI Technology. In an effort to keep one step ahead of third-party vendors offering process-independent tools, the company has just introduced its fourth-generation ASIC design system, called V8. The system tightly integrates tools for automatic logic design, test, physical design, and factory interface, says Doug Fairbairn, vice president and general manager of the ASIC Division.

Two key elements are the Logic Assistant and the Test Assistant. The first, says Fairbairn, is an expert system that melds on one tool architectural design analysis and partitioning, silicon compilation, logic synthesis, chip sizing, and power estimates. Test Assistant helps the designer isolate blocks to be tested, insert isolation circuitry, and generate test programs.

The company has also introduced two new advanced floor planners: Gate Assistant, which generates floor plans for VLSI Technology's 1.0- and 1.5-μm 100,000-gate channelless arrays, and Chip Assistant, which generates floor plans for cell-based designs.

A new niche market that many manufacturers are eyeing with interest is mixed analog/digital ASICs. Traditionally the domain of specialized ASIC houses, this market is expected to surge to $450 million in 1993 from $112 million last year, says market watcher ICE. Sierra Semiconductor Corp., a mixed-mode pioneer, estimates that at least 40% of its new standard-cell designs this year will be analog/digital. By 1993, ICE expects cell-based methods to predominate, accounting for $390 million in sales.

With such growth potential, it's no wonder that major ASIC houses such as LSI Logic, National Semiconductor, and TI are making big plans. LSI Logic has just introduced its LAD310 biCMOS analog/digital array (see p. 67), while National is going after the high-performance end of the business with its customized-linear ASIC, or CLASIC, program. This standard-cell effort is now based on National's proprietary linear bipolar process, LFast; biCMOS will be added next year. Meanwhile, at TI, a proprietary advanced linear design system can build mixed analog/digital circuits using any of the linear processes.

A major effort is under way at Cadence to develop tools for analog and mixed-mode circuits. Its new Analog Division next month will unveil its first product: Artist, an analog custom-IC design system. Artist incorporates an analog design and capture tool and symbol library, analog core simulators, integrated layout and verification tools, software for parasitic capacitance extraction and resimulation, and an advanced statistical analysis tool.

With all the excitement surrounding CAD, it's no surprise that design automation companies are flourishing. The demand for more sophisticated third-party software is leading CAD houses to a 30% growth spurt this year, ICE says. In logic synthesis, sales should reach $265.4 million in 1992, against $39.3 million this year, says the Technology Research Group.

Three companies have just released new synthesis tools. Silicon Compiler Systems Corp. in San Jose is the first to provide mixed analog and digital circuit synthesis and layout (see p. 62). Rival Synopsys has introduced the latest versions of its synthesis tools Design Compiler and HDL Compiler. Design Compiler can now synthesize state machines, a capability that marketing manager Robert Dahlberg claims produces circuits that are 15% smaller and 5% faster than before (see p. 108).

VLSI Technology this month announced the ASIC Synthesizer, a tool that eventually will automatically synthesize a complete ASIC from a Verilog or VHDL behavioral description. The first version creates a gate-level design, much like the HDL Compiler from Synopsys. But the next version, set for release in mid-1990, will recognize data paths in a VHDL or Verilog description, says Michael O'Brien, marketing manager. Instead of synthesizing a gate-level equivalent, it will call VLSI Technology's data-path compiler, which will produce an implementation that is tens of nanoseconds faster and at least a third smaller than a synthesized gate-level implementation. Also, the tool will recognize every data path in a larger VHDL or Verilog description and share data paths among multiple functions to reduce circuit size. The final version, due by the end of next year, will recognize memory as well.

Meanwhile, some CAD companies are restructuring for improved efficiency. Among them is Silvar-Lisco Corp. of Sunnyvale, Calif., which has sold portions of refocused on particular markets (see story at right). ☐

CAN SILVAR-LISCO TURN ITSELF AROUND?

After several quarters of almost crippling losses, a new management team has steered Silvar-Lisco to a modest profit—$41,000 on sales of $3.7 million—in its first quarter, ending June 30. But it remains to be seen whether the Sunnyvale, Calif., computer-aided-design house, now that it's scaled-down and refocused, can capture enough of the CAD market to stay healthy.

Founded in 1981 with the merger of two companies, Silvar-Lisco chalked up steady sales growth but wasn't turning a profit. Sales peaked at about $26 million in 1987, but by the end of the company's fiscal year in April 1988, sales had fallen to $19.9 million with a net loss of $11 million.

The problem was a lack of focus, says Peter Bagnall, vice president of marketing and one of the management team brought in to turn the company around. Being a fully integrated supplier of complete design systems is not necessarily the best way to achieve long-term growth, Bagnall says.

Silvar-Lisco has withdrawn from the market its analog-design and printed-circuit-board layout tools to concentrate on its specialties: physical layout and design verification, supported by enhancements to its design-capture and behavioral-simulation products.

The company has unleashed a blitz of new products, including the SDSi, a user-friendly schematic-capture system; an updated version of its SC-II cell-based layout software; Princess, a full-custom integrated circuit layout editor; and Avant-Gards, a new version of its gate-array router, timer, and synthesis tool.

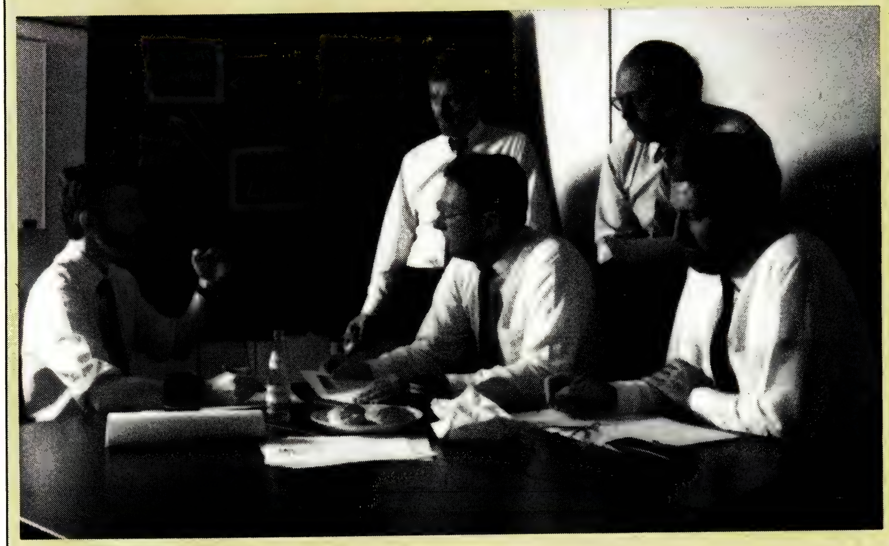
The refocusing was combined with a significant downsizing. The elimination of several product lines led to the laying off of 75 employees. The company also moved from Menlo Park, Calif., to smaller quarters in nearby Sunnyvale. And it transferred its European development activities to a new corporation jointly owned with Silicon Compiler Systems Corp. of San Jose, Calif.—the European Development Corp., which is working on analog and mixed-signal CAD tools.

Silvar-Lisco's aim now, Bagnall says, is "to be the leader in specific design software focused on physical layout and design verification; and I think our new [product] releases indicate that we have clear technical leadership over the competition in those areas."

Silvar-Lisco is sufficiently confident that it has brought losses under control and found the right formula for future growth, says Bagnall, that it has discontinued a search for a merger or consolidation. In this respect, he says, it is ahead of many CAD competitors that have been forced down that road.

"The only other alternative to survival is to do what we have done—downsize the company and focus our product strategy," says Bagnall. "It was a choice between being lean, mean, and competitive, or fat, broke, and out of business."

The company still has a way to go. Peter Schleider, a partner at the investment firm of Wessels, Arnold & Henderson in Minneapolis, isn't impressed with the latest financial news from Silvar-Lisco. He says that the company's technology is old and that its current financial condition is due more to the selling off of assets than to a significant sales boost. The company has stopped the bleeding, Schleider says, but now it must get its new product development effort in gear to succeed in the competitive CAD arena. *–B. C. C.*



The managers who are working to turn around Silvar-Lisco are (from left) Guido Arnout, Phil Nutburn, Sam Hedgpeth, Peter Bagnall, and Tony Wainwright.

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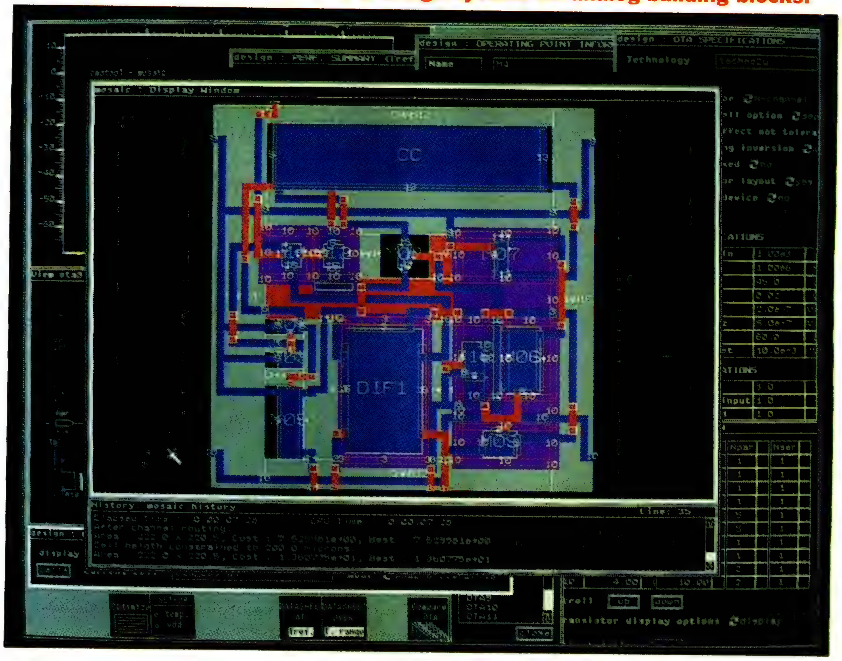
SCS's Explorer AutoLinear is a design system for analog building blocks.



ANALOG GETS AUTOMATED

Silicon Compiler Systems offers the first circuit and layout synthesis tools for analog and mixed-signal devices

Designers of analog and mixed-signal integrated circuits finally have access to powerful computer-aided-design tools, thanks to the arrival of two new synthesis products that put them on an equal footing with digital designers. The new offerings, from Silicon Compiler Systems Corp. of San Jose, Calif., are the first commercially available circuit and layout synthesis tools for analog and mixed-signal ICs.

SCS claims that its Explorer AutoFilter and Explorer AutoLinear products give analog and mixed-signal IC designers the automated design help previously available only to designers of digital chips. Automation of analog design has been slow to develop primarily because of the complexity of the process. Analog design involves a large number of interrelated specifications that must be met for an analog function to perform as desired. Typically, these could include gain, bandwidth, slew rate, 1/f noise, and common-mode rejection ratio.

Up to now, analog designers relied on a combination of manual and semiautomated steps using software developed either by themselves or by university labs, according to Steve Eichenlaub, SCS product marketing manager. Of the other alter-

BY SAMUEL WEBER

natives to custom designs, he says, “analog arrays deliver relatively low performance and provide limited design flexibility, and analog standard cells are effective in many cases but often fall short of containing the full complement of structures required for a custom design.”

Each of SCS's new offerings incorporates the key aspects of analog synthesis, including design, optimization, and analysis. With Explorer AutoFilter and Explorer AutoLinear, designers can rapidly produce accurate schematic, simulation, and layout views of desired analog functions simply by specifying desired levels of key parameters.

SCS's new additions to its Explorer series come at a time when demand for mixed-signal designs is growing. The Technology Research Group, a Boston-based market research firm, predicts that the number of IC designs having some degree of analog content will rise from 3,000 in 1988 to 20,000 in 1991—or 40% of all IC designs.

These tools let designers turn out accurate views of analog functions simply by specifying key parameters

SCS is aiming its new tools at vertically integrated companies and at suppliers of application-specific ICs to the telecommunications, automotive, and consumer-electronics industries.

Explorer AutoFilter provides a unified design environment that encompasses all the key steps in designing switched-capacitor filters. With AutoFilter's graphic filter-performance capture, embedded synthesis algorithms, and automated layout facilities, designers can synthesize a filter from initial response specification to process-specific layout in less than an hour on a high-performance work station, SCS claims. Using conventional design tools, the process takes days or sometimes weeks.

As with other SCS software, designers interact with the tool through an object-oriented graphical interface that lets them choose from five different screen presentations. Designers can accept default values for a variety of specs and trade-offs and proceed to the next screen, or they can modify key variables, specify acceptable ranges, or select trade-off paths to follow.

The first step in the Explorer AutoFilter process is filter synthesis. In this step, designers enter specifications for the desired filter (high-pass, symmetrical bandpass/bandstop, or nonsymmetrical bandpass). They can specify key performance variables, such as cutoff frequency, ripple, gain, rejection, sample frequency, and filter-approximation type (Butterworth or Chebychev, for example). AutoFilter then automatically synthesizes the z-transform H(z), calculates the filter degree, and displays filter magnitude, gain, phase, group delay, and loss as a function of frequency. Designers can exercise trade-offs in original specifications.

In the second step, a screen displays the results of the synthesis in more detail, including poles and zeros in the complex plane, as well as magnitude, group delay, and phase information. Poles and zeros can be added, moved, or deleted to create a specialized response. The impact of these changes is promptly displayed on the screen for interpretation, modification, and acceptance.

With the next three screens, the methodology becomes more specialized. In the third step, the synthesis proceeds from a mathematical representation of a filter network to an electrical representation, in which the z-transform for the filter is implemented using a switched-capacitor network based on cascaded biquad topologies. These are a wide variety of general purpose topologies developed at AT&T Co. Results of this step are displayed in a combination of text and graphics, including schematics for each of the synthesized biquads and such detailed specifications as capacitor array size, operational amplifier bandwidth, op amp loading, and individual capacitor sizes.

In the fourth step, network optimization takes into account such real-world issues as component sensitivity to the manufacturing process. For example, numerical optimization algorithms can be invoked to adjust individual capacitor values so that the filter response remains within specifications over the full range of specified capacitor ratio mismatch.

The fifth step involves synthesizing the layout. With the Switcap file format, any switched-capacitor circuit—including biquad, ladder, filter, and data converter—can be input. The output is a process-specific layout of the switches, capacitors, and op amps.

The synthesized layout takes the form of a rectangular block, with the op amps in a row across the top, the capacitor array in the middle, and the switches at the middle or bottom. AutoFilter gives the designer control over power and signal line widths, capacitor and switch topologies, and signal and clock router types. SCS's GDT Designer allows full viewing and editing of layouts; industry-standard formats (GDSII, Spice, or Switcap) are available for use with other vendors' layout tools.

Explorer AutoLinear is an integrated design, optimization, and analysis tool that allows designers to create analog building blocks for an analog or mixed-signal chip, including operational transconductance amplifiers (OTAs), op amps, comparators, voltage references, current references, resistors, capacitors, transistors, and crystal oscillators.

Although Explorer AutoLinear features the same degree of automatic synthesis from high-level specifications to process-specific layout as AutoFilter, designers can intervene and influence the synthesis at intermediate stages. For instance, an OTA design may be implemented by specifying only the gain and bandwidth. AutoLinear then assumes default values for such key parameters as slew rate, 1/f noise, and current mirror ratios and determines the device parameters required for the chosen circuit topology.

If the chosen topology doesn't meet the performance specs, AutoLinear guides the designer in modifying the design. An analysis mode lets the user modify and optimize the cell parameters. “If the user decides, ‘I'm a better analog designer than your software,’ he or she can go in and influence the trade-offs,” says Eichenlaub. “We recognize that every analog design has to be at least scrutinized by an analog designer.”

Designs can be viewed graphically and in text form. The widths and lengths of transistors and Spice parameters for each component are provided. A graphical window displays relationships between key variables or annotated circuit schematics.

AutoLinear then synthesizes a process-specific layout. Placement of circuit elements takes into account component matching and noise sensitivity; the program then proceeds with a coarse/fine autorouting algorithm based on simulated annealing. In minutes, AutoLinear produces a block layout that accommodates specified constraints such as block height, connector locations, and component locations. A robust set of editing features lets designers intervene in the process. AutoLinear's output is available as an SCS layout data base, a GDSII or CIF layout data base, or a Spice netlist.

AutoLinear and AutoFilter are the result of partnerships between SCS and two other companies: Centre Suisse d'Electronique et de Microtechnique, a Swiss developer of analog synthesis tools, and International Microelectronic Products Corp. of San Jose, a supplier of mixed-signal ASICs. Both partners will work with SCS to develop next-generation analog and mixed-signal synthesis products.

AutoLinear and AutoFilter are installed at beta sites and have already produced successful chip designs, according to SCS. They will be available for distribution worldwide next month. Pricing begins at $40,000 on Sun Microsystems Inc. Sun 3 or Apollo Computer Inc. DN4500 work stations. □

Sizing Up the Earth in 200 B.C.

Eratosthenes believed the earth was round. As director of the great library at Alexandria in Egypt, he decided to go beyond abstract argument and actually measure it to back up the argument.

Knowing that the midsummer noon sun shone straight down a vertical well in Syene far to the south, he measured the slight angle of the sun's shadow in Alexandria on the same day. He figured the distance between the two cities by how long it took a camel to walk there. Then, with a little simple geometry, Eratosthenes came up with fairly accurate figures for the earth's circumference and radius. His pioneering measurement made a significant impact on history.

Eratosthenes

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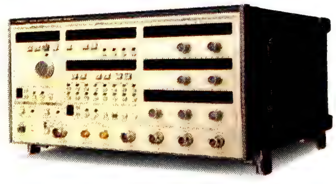

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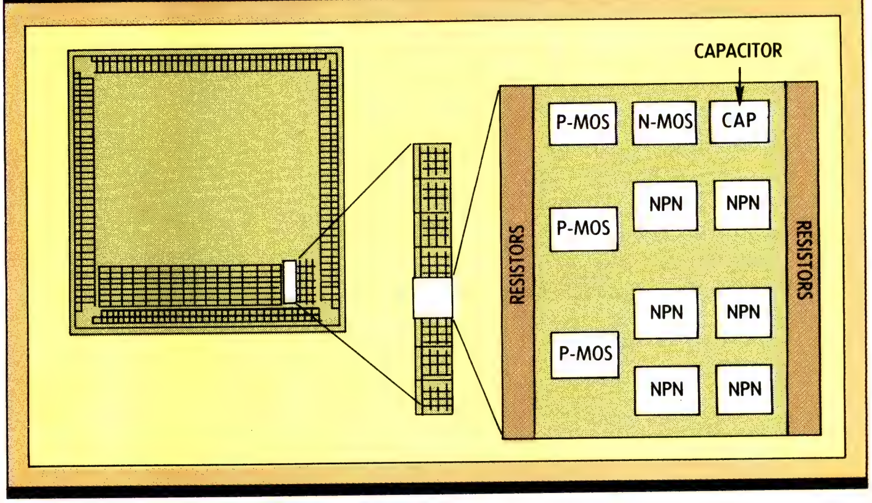
BY BERNARD C. COLE

MIXED-MODE MAGIC IN ASICs

HOW THE LAD310 IS PUT TOGETHER



In LSI Logic's LAD310 series, each analog tile contains the elements shown in the blow-up. The biCMOS parts combine high gate density with a range of analog functions.

In the race to provide mixed-mode application-specific integrated circuits that meet the often conflicting needs of users, a new leader has emerged. The LAD310 series from LSI Logic Corp. represents the most ambitious attempt to date to satisfy the growing demand for more powerful mixed-mode ASICs.

Up to now, vendors of mixed-mode ASICs haven't found a way to meet the demands of all users. Devices manufactured in CMOS provide relatively high digital gate densities but only a small amount of relatively low-performance analog power. Bipolar devices offer much higher analog performance and density but, because of power dissipation, a fairly meager digital gate count.

The LAD310 series, fabricated with a 0.9-μm biCMOS process, combines high gate density and an extremely wide range of analog functions. The series includes seven circuits, ranging from 1,512 gates and 96 analog tiles in the smallest version to 114,987 gates and 672 tiles in the largest. The digital CMOS circuitry cuts delays to 570 ps for a two-input NAND, while the bipolar analog transistors have a current gain of 80 and toggle frequencies as high as 6.5 GHz.

Key to the high performance and high density is the use of a biCMOS structure, says David Baillie, director of ASIC marketing for the Milpitas, Calif., company. Polysilicon is used for both the CMOS transistor gates and the bipolar transistor emitters. The actual emitter base junctions, he says, are formed from the polysilicon using an advanced rapid thermal annealing technique.

For the analog functions, LSI Logic deploys passive components, such as resistors and capacitors, for the circuit designer. Most analog-array vendors provide a range of fixed resistors and capacitors that are connected in series and/or parallel to achieve the values needed. According to Baillie, this approach requires excessive die area and poses matching difficulties. While the absolute values of the resistance or capacitance achievable using this approach are reasonable, it is difficult to achieve a tight tolerance if several components need to be matched in value, he says.

To overcome these problems, designers at LSI Logic used what the company calls programmable passive components. By using polysilicon material as the top electrode of a capacitor and as the uncommitted resistor area, Baillie explains, LSI's designers were able to program the actual value of each resistor and capacitor with only one additional mask step.

This approach also simplifies component matching because the affected devices can be configured to be topologically equal.

The resulting analog array consists of a number of tiles, each of which contains six npn transistors, two pairs of 5.0-μm p-channel transistors, a pair of 1.5-μm p-MOS transistors, a pair of 1.5-μm n-channel transistors, a number of fixed-value resistors, and programmable areas for resistors and capacitors.

Because LSI Logic designed the digital section of the LAD310 series to be identical to the company's LCA10000 series, an extensive library of digital functions is available. In addition, more than 25 analog library functions have been incorporated, including operational amplifiers, comparators, references, multiplexers, and analog-to-digital and digital-to-analog converters, all of which are accessible through the company's Modular Design Environment.

The ability to fabricate 6.5-GHz bipolar transistors makes it possible for the LAD310 to produce an op amp with a 600-MHz bandwidth or one with offset voltages as low as 2 μV. Because of the high speed of the bipolar transistors, video-speed flash converters can be implemented very easily, Baillie adds. □

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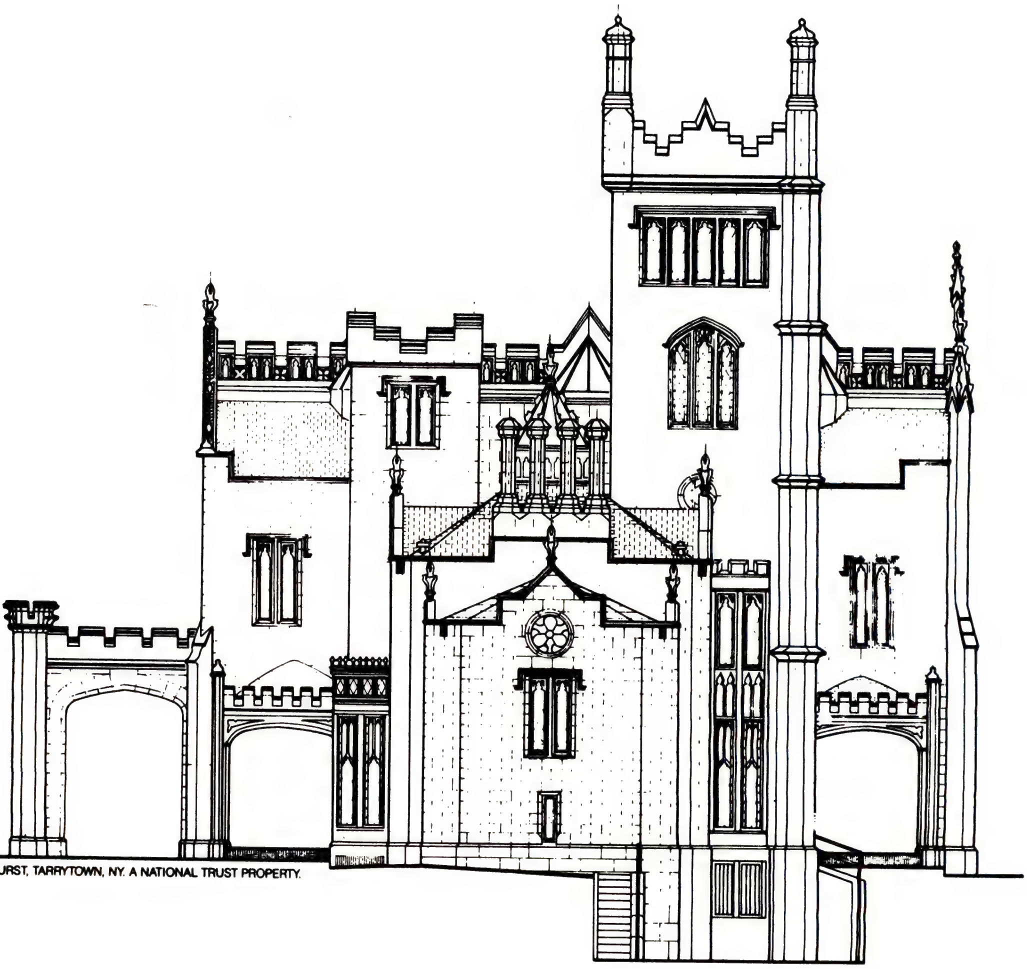

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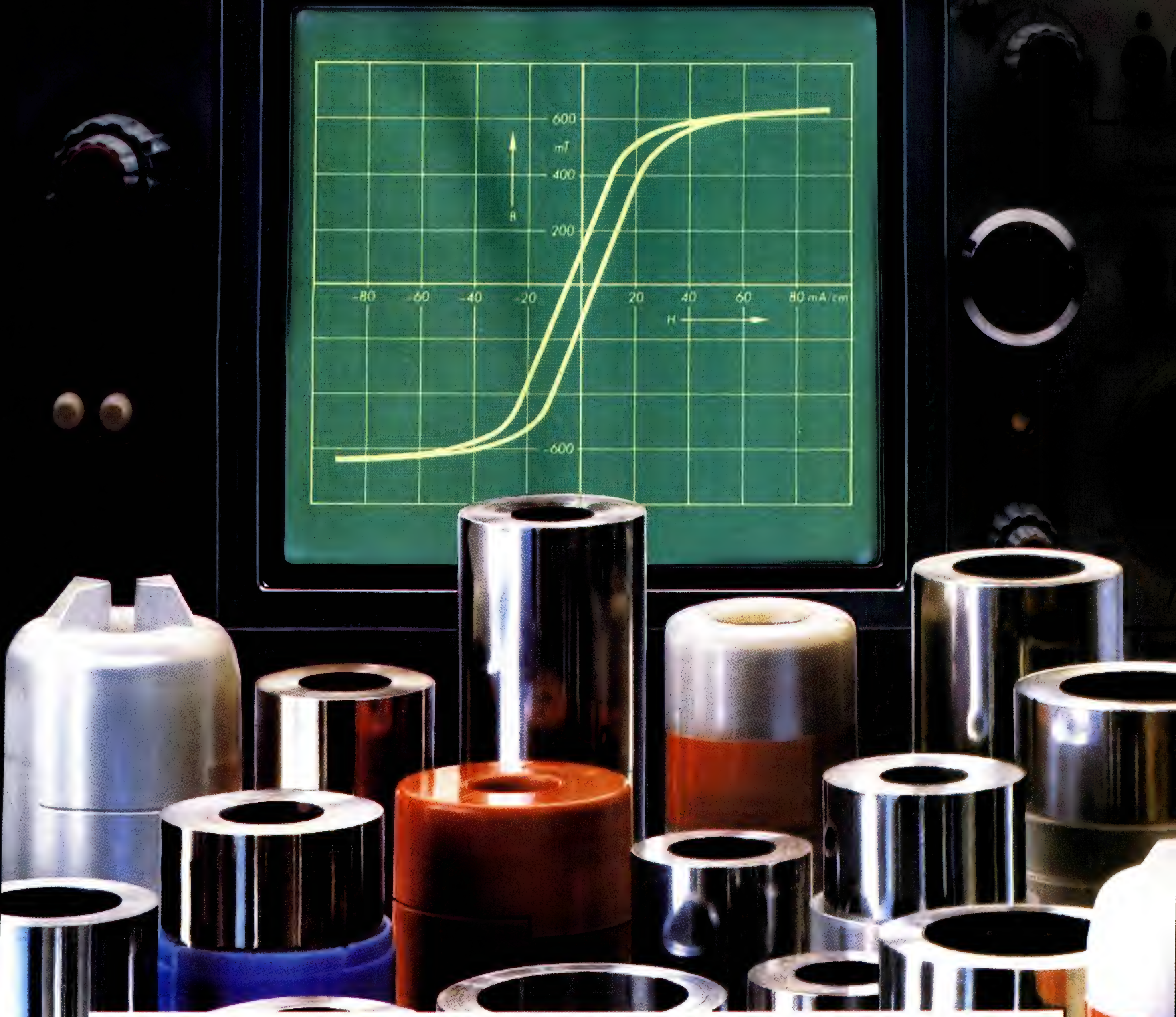

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Circle 109

Trading Places: How the U.S. Is Fighting Back

BY JACK SHANDLE

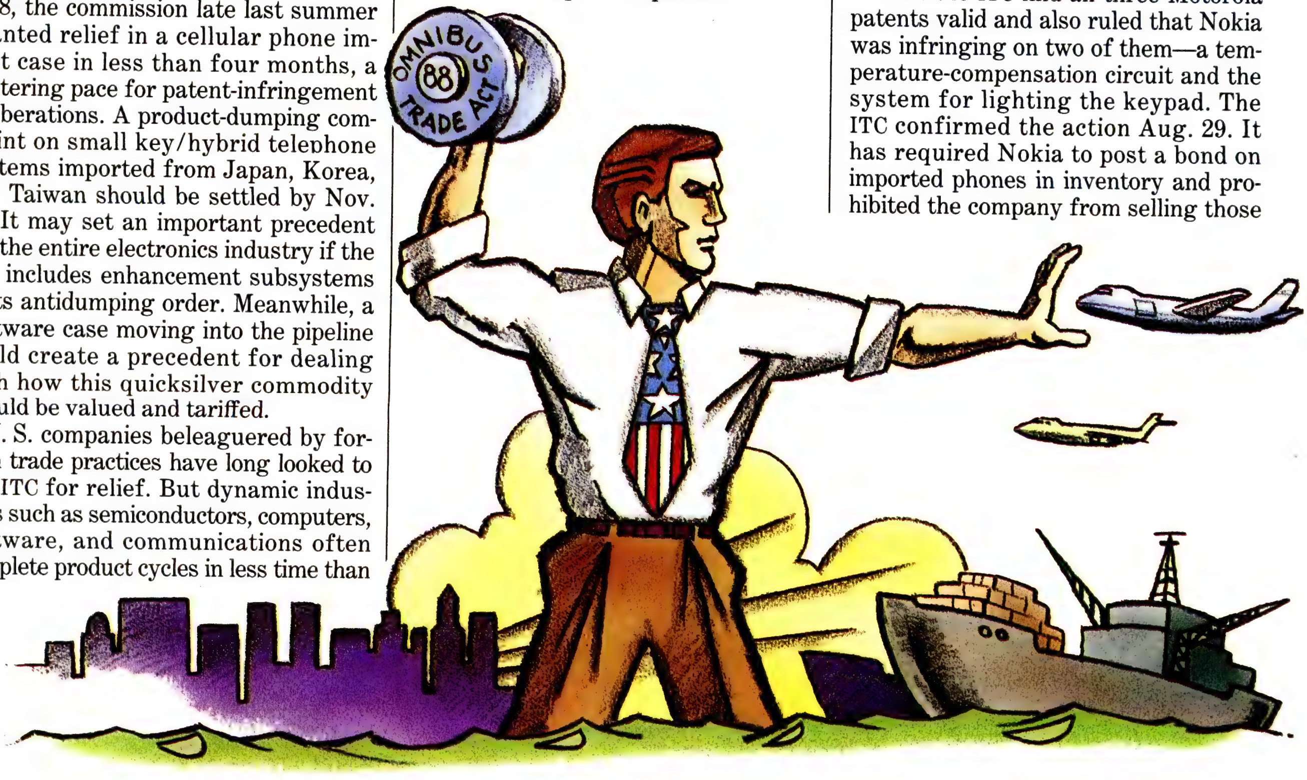
Two world wars and a silicon revolution after it was founded in 1916, the U. S. International Trade Commission is finally becoming a potent force in the conduct of international business for fast-moving technologies such as electronics, software, and communications.

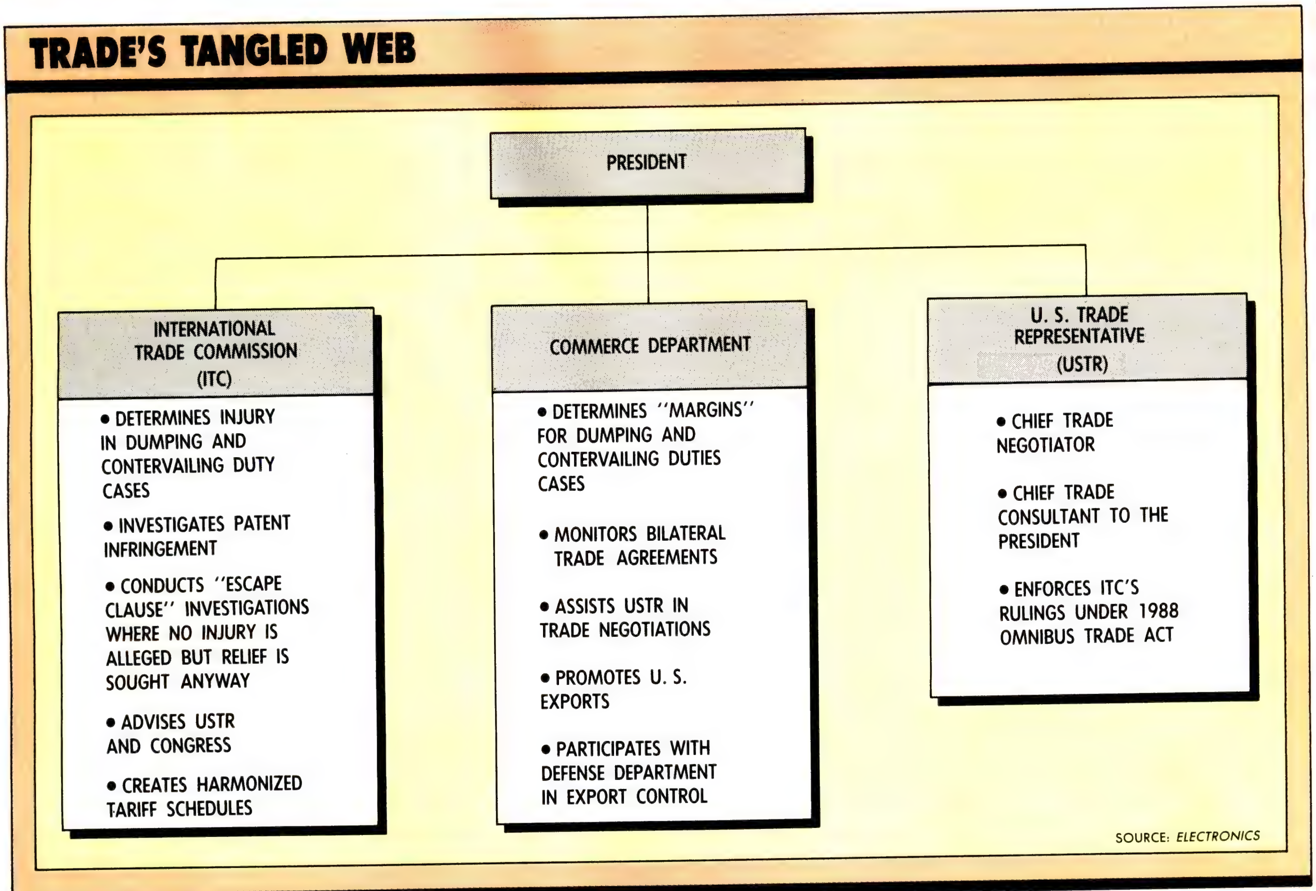
News from the ITC is coming fast, and most of it is good for U. S. companies. Using expedited procedures enacted in the Omnibus Trade Act of 1988, the commission late last summer granted relief in a cellular phone import case in less than four months, a blistering pace for patent-infringement deliberations. A product-dumping complaint on small key/hybrid telephone systems imported from Japan, Korea, and Taiwan should be settled by Nov. 24. It may set an important precedent for the entire electronics industry if the ITC includes enhancement subsystems in its antidumping order. Meanwhile, a software case moving into the pipeline could create a precedent for dealing with how this quicksilver commodity should be valued and tariffed.

U. S. companies beleaguered by foreign trade practices have long looked to the ITC for relief. But dynamic industries such as semiconductors, computers, software, and communications often complete product cycles in less time than it once took for the ITC to act. "It doesn't take long for an offshore manufacturer to blow out a U. S. competitor," says Carl Silverman, Intel Corp.'s general counsel for intellectual property. "Look what happened with DRAMs [dynamic random-access memories]."

Last year's Ominibus Trade Act has changed that. A hint of how the future will shape up came last April when Motorola Inc. asked the ITC for a temporary exclusion order against Nokia Mobira Inc. to stop the importation of cellular phones that Motorola claimed were infringing on seven of its patents. Based in Largo., Fla., Nokia Mobira is the U. S. subsidiary of the $3 billion Finnish electronics giant Nokia Oy. As the first company to use ITC's stepped-up procedures, Motorola asked the commission to immediately consider three key patents, with the other four to wait for a full-blown hearing.

By Aug. 9, an administrative law judge assigned to the case recommended that the ITC find all three Motorola patents valid and also ruled that Nokia was infringing on two of them—a temperature-compensation circuit and the system for lighting the keypad. The ITC confirmed the action Aug. 29. It has required Nokia to post a bond on imported phones in inventory and prohibited the company from selling those




TRADE'S TANGLED WEB
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U. S. TRADE REPRESENTATIVE (USTR)
• CHIEF TRADE NEGOTIATOR
• CHIEF TRADE CONSULTANT TO THE PRESIDENT
• ENFORCES ITC'S RULINGS UNDER 1988 OMNIBUS TRADE ACT

SOURCE: *ELECTRONICS*

The ITC interacts with both the Commerce Department and the U. S. International Trade Administration. For example, after the ITC determines that foreign trade practices are injuring a U. S. industry, Commerce sets the countervailing duty.

models pending the full hearing on all seven patents. This should be finished next March under the accelerated timetables imposed by the Omnibus Trade Act. Although Motorola limited its comment to an official press release, the Schaumburg, Ill., company was clearly pleased that the tables had been turned so quickly.

"The new timetable reduces to about 90 days what used to take at least nine months," says Intel's Silverman. Besides the compressed time frame, U. S. companies no longer have to prove injury in the expedited proceedings. "Together, it makes preliminary relief a lot more do-able," Silverman says. "Proving injury required a lot of paperwork and litigation time."

Predictably, foreign exporters are not as enthusiastic. "We feel that we didn't have sufficient time to tell our story under the expedited proceeding," says Nokia president Jan Loeber. "It's very fast. It's designed to help an American company out. We think the court proceeding coming up will give us time to tell our total story." Meanwhile, deeper rumblings are being heard in Europe, where some companies have alleged that the new ITC procedures violate the General Agreement on Tariffs and Trade. Sources at the Geneva-based trade organization say that the Omnibus Trade Act procedures could be interpreted as violations of GATT.

Among these is a procedure empowering the U. S. Trade Representative to take retaliatory action after the ITC determines that systemic trade practices are harming U. S. access to overseas markets. The problems with this are twofold, the Europeans say. The retaliatory measures may be inconsistent with GATT policy holding that member nations must be treated in nondiscriminatory ways. In addition, complaints by one country against another can lead to bilateral negotiations, a violation of GATT's multilateral-negotiations rule. "The U. S. is, in effect, setting itself up as judge and jury," says one source.

The second problem concerns imports that may violate a U. S. patent—and the ITC's new power to stop such imports quickly with a temporary exclusion order. The European Community contends this procedure gives foreign goods less favorable treatment than U. S. goods, which might also be infringing a U. S. patent—but are obviously not subject to a temporary exclusion order. The EC has filed a complaint on this issue with GATT.

The Motorola vs. Nokia case was the first in which the ITC granted a temporary exclusion order. But a dumping case pitting AT&T Co. against numerous Japanese, Korean, and Taiwanese companies is likely to make just as big a splash. AT&T and Comdial Corp. of Charlottesville, Va., have charged product dumping against the exporters of key/hybrid telephone systems that are typically used by small companies.

A final decision was expected late last month, but the ITC's preliminary findings leave little doubt that countervailing duties will be levied against the Far Eastern companies, says Eric Nelson, research director for the North American Telecommunications Association, a Washington trade group.

Prices of key/hybrid systems will rise 10% to 15% after the ruling, says Nelson. Over the long term, large Japanese companies will move manufacturing into the U. S. to avoid the duty. Smaller companies that cannot afford to do so may drop out of the market. Observers are also looking at the AT&T-Comdial decision to set a far-reaching precedent on how enhancement products will be handled. The key/hybrid systems themselves are not big profit makers, says Nelson. But the enhancement boards and subsystems for them are. If the ITC's dumping order includes enhancements, he says, it will likely set a precedent for other add-on products across all electronics-industry systems.

An important issue unrelated to the AT&T-Comdial decision concerns the act itself. "It is very fuzzy in some areas," says Nelson. For example, though the act says foreign nations should live up to the spirit of previous trade agreements, it does not have a specific set of processes in place to monitor and enforce them. Take the U. S.-Japan Semiconductor Agreement. It "is probably being monitored in an informal way, but no one knows what will happen if the Japanese do not live up to the spirit of the agreement," Nelson says.

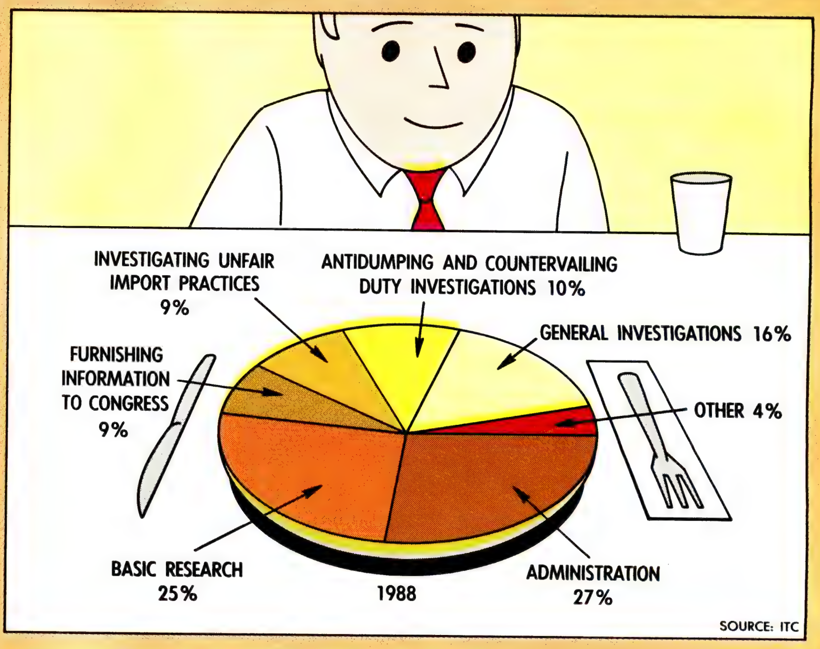
Sanford L. Kane, president of the recently formed U. S. Memories Inc. DRAM consortium, has already expressed concerns about the law's unrefined nature [*Electronics*, September 1989, p. 47]. And Intel's Silverman believes the ITC may not have the manpower needed for vigorous enforcement. "It takes an investigating attorney or two to represent the government in these proceedings," he says.

Enforcing exclusion orders also demands manpower. After Intel obtained a temporary exclusion order against design houses that were trying to piggyback on a foreign fab's patent licenses, says Silverman, the Santa Clara, Calif., company discovered the products were still coming in. "Although it's the Customs Department's responsibilty, "there's still a question of whether the ITC has the manpower to make sure its orders are being enforced," he says.

Software always seems to create special legal problems, and trade issues are equally thorny. The question of importing software may not be a burning one today, but that could change, says Cedric Nash, international sales manager for Visible Systems Corp. of Waltham, Mass. "Right now, the U. S. exports far more software than it imports," he says. "But there are many highly coordinated efforts, particularly in Japan, to write leading-edge software. What's going to happen when they come to fruition?" Visible Systems, which specializes in tools for computer-aided software development, has filed a complaint with the U. S. Commerce Department to stop Computer Systems Advisers Pte. Ltd. from exporting a CASE tool called POSE. Because POSE was developed under a government subsidy, says Nash, the Singapore-based company can set an artificially low price.

The case will eventually wind up before the ITC, says commission spokesman Jim Craig, but first the Commerce Department must determine the dollar amount of the subsidy. The ITC determines whether a U. S. industry sustained injury as a result of a subsidy and determines a remedy, which in many cases would be a countervailing duty.

WHAT'S ON THE ITC'S PLATE



SOURCE: ITC

What will happen when foreign efforts to write leading-edge software bear fruit?

Therein lies the rub for software developers. Software is tariffed on the value of the media—not the intellectual property. "Commerce forewarned us a little bit," says Nash. "Even if it determines that a subsidy situation exists, the government may be powerless to do anything about it." Typically, products can be held until the duty is paid. But software doesn't get imported in the hold of a ship or as air cargo. It enters electronically over a modem or in somebody's suitcase on floppy disks.

The Visible Systems' complaint could open a Pandora's box of trade retaliation, says Sherman Drusin, president of Computer System Advisers Inc. in Woodcliff Lake, N. J., the Singapore company's U. S. subsidiary. "The U. S. government, especially the Department of Defense, is probably the biggest subsidizer of software in the world," says Drusin. Standard language in DOD contracts reduces to the fact that "except for security-sensitive and space applications, the only stipulation generally is that the federal government can use it at no cost," he says.

Another hurdle in Visible Systems' path is GATT's approach to software. "Import duties are assessed only on the media," says Alice Denson, manager of international affairs at the Association of Data Processing Service Organizations. The Alexandria, Va., group—an association of software developers that includes both U. S. firms and subsidiaries of foreign companies—has no policy regarding GATT's approach. "There is no legislation kicking around in Congress that might challenge the GATT approach," she says.

GATT gives its 97 member countries two options for tariffing software, says a source in Geneva. Although most industrialized countries calculate tariffs only on the value on the medium, developing countries such as India and Brazil generally calculate their duties on the intellectual property residing on the disk or tape. GATT doesn't tell its members how much duty to charge, but it does insist on a policy of nondiscrimination, says the source. That is, a member nation must impose the same duty percentage on the product regardless of its origin. Within the European Community, there are no duties on software and no strong sentiment to change present GATT policy.

Additional reporting by John Gosch

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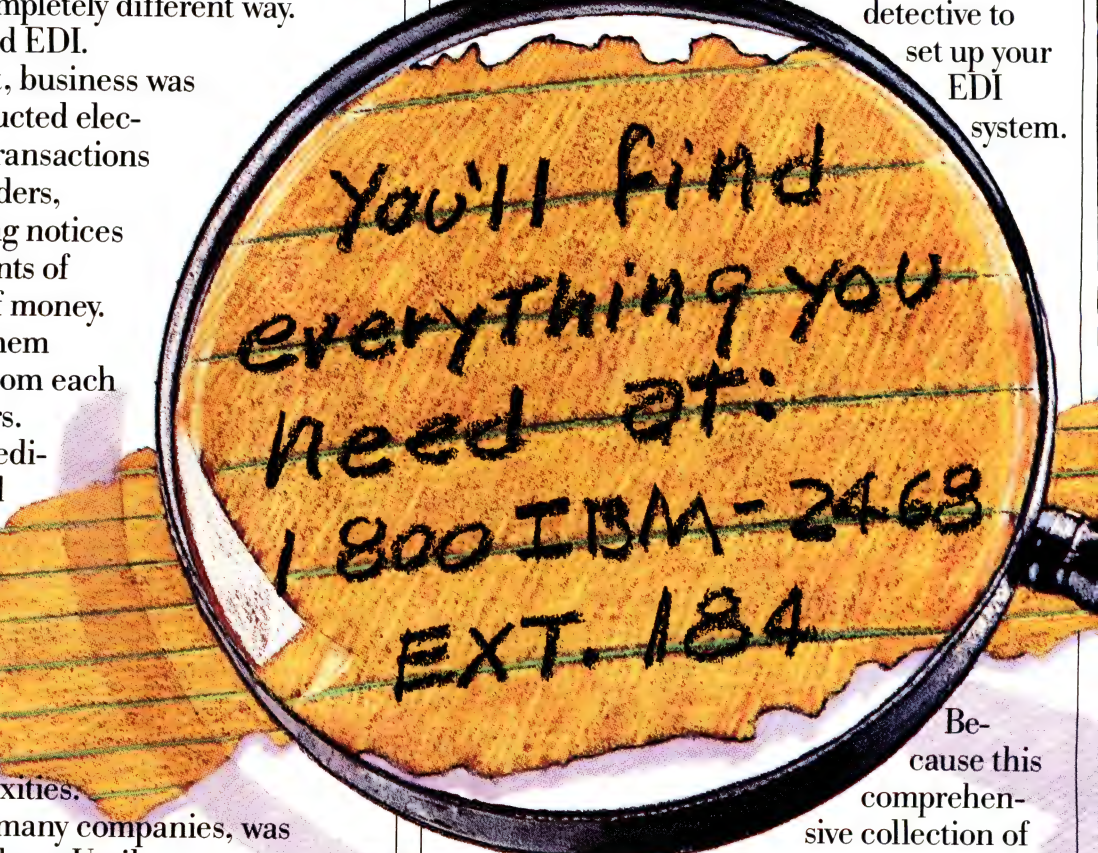
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BRINGING DOWN THE COSTS OF ATE

ATE vendors are playing all the angles in an effort to give customers what they want: powerful test systems at affordable prices

◆

Makers of automatic test equipment are hoping to break out of a collective slump by giving customers what they have long clamored for: alternatives that help lower the cost of testing.

GenRad's new GR2276 Manufacturing Process Analyzer finds bad ICs.

ATE vendors are adopting a number of product strategies in their quest for more affordable systems. Among the options now available are device tester handlers that accommodate up to 64 chips at a time, systems that test devices on wafer instead of as packaged parts, and systems that cut the time it takes to test, even by seconds. Test equipment based on CMOS technology offers the speed and accuracy of much pricier systems built with emitter-coupled-logic technology.

Meanwhile, component ATE systems with built-in scan testability circuits promise to slash test costs—from $10,000 per pin down to $1,500. Board testers are reducing test time and costs with handling equipment that automates the mounting and unmounting of boards. And testers priced at under $10,000 are available for a limited range of boards.

The move toward lower-cost testing options has already paid off big for one ATE vendor. Megatest Corp.'s low-cost testers have propelled the San Jose, Calif., company to a 30% growth rate in the past two years. Meanwhile, the ATE market in general has been in the doldrums. Business is off by 5% this year, according to Kenneth Neff, vice president of Prime Data, a market research firm in San Jose. He pegs the ATE market at $2 billion in total 1989 sales, with $1.2 billion coming from sales of component ATE and $600 million from board testers.

Prime Data projects a modest upturn—growth of 5% to 10%—for the ATE business next year, with steady increases over the next few years. By 1993, the market will reach $3.3 billion, the market researcher predicts, with sales of component ATE reaching $2.1 billion and board testers $900 million.

To reach those levels, ATE vendors will have to make an all-out effort to woo customers with lower-cost options. This is especially true for makers of component ATE systems; in this market, the integrated circuits being tested are under continuing cost-performance pressure. Testing now ranks as a large factor in the cost of an electronic component.

ATE gear that tests more devices in parallel can help

BY JONAH McLEOD

Semiconductor Test Solutions' STS5000 mixed-signal tester offers high-speed testing for ISDN devices.

lower costs for users. "Testing a high volume of memory chips per hour is the key to success in this business," says Jim Mulady, manager of sales and marketing for the IC Tester Division of Ando Corp. in Sunnyvale, Calif. "We have gone through the generations of 10- and 25-MHz memory testers and are embarking on the 50-MHz generation." The emergence of 1- and 4-Mbit dynamic random-access memories as well as faster static RAMs has created the need for this class of tester, he says. Ando's new 50-MHz 8045 memory test system can be connected to four Ando 710 handlers to test 64 memory devices at a time.

Parallel testing is not restricted to memory chips. The T3382 100/200-MHz VLSI Logic Test System from Advantest America Inc. of Lincolnshire, Ill., features 512-pin test capability and comes with a surface-mounted-device dynamic handler, the M4132A, that can handle quad flat packs, pin-grid arrays, and various chip-carrier packages and flat-package devices. The M4132A can handle two devices at a time and can sort devices into three classes.

Testing of packaged parts has become more expensive than testing individual components, especially for application-specific ICs with high pin counts. One way to lower the cost of testing is to perform full characterization tests at wafer probe, says Steve Bisset, president of Megatest. New "membrane-probe" technology makes it possible to achieve sufficient impedance control on the wafer even for devices with very high pin counts, Bisset says.

One obstacle to full characterization testing at the wafer level has been the use of dyes to mark bad devices. When wafers were tested at high temperatures, the dyes would melt and run, making it difficult to find faulty devices later. Integrated manufacturing facilities now keep track of each die on a wafer in a manufacturing data base. Bad dice are marked in the data base rather than with dyes on the wafer itself.

But the way is not entirely clear for widespread characterization testing at the wafer stage, Bisset cautions. Users need probers that can handle multiple dice at a time and that can accommodate more than one type of ASIC device on a wafer, he says.

Systems that reduce testing times for individual devices can also help cut user costs. The STS5000 mixed-signal device tester from the Axion Division of Semiconductor Test Solutions Inc. provides high-speed testing for integrated services digital network devices, according to the Burlington, Mass., division.

The STS5000, the newest member of a product family that also boasts the STS3000, features an array processor rated at 20 million floating-point operations per second that can perform a sigma-delta converter test for an ISDN chip in 3 seconds, shaving 0.2 seconds off the competition's best time, according to Rene Verhaegen, director of marketing at Axion. Priced at $400,000, the STS5000 is less expensive than engineering evaluation systems such as the A500 from Teradyne Inc. of Boston and the Synchromaster from LTX Corp. of Westwood, Mass. Axion's new offering runs ISDN transmit- and receive-frequency tests simultaneously instead of one at a time—a feat that Teradyne's A500 can't match, Verhaegen says. Teradyne has announced a new version of the A500 for testing discrete devices called the A510AL (see p. 85).

A major contributor to the rising cost of testing has been the adoption of a per-pin architecture in test systems, introduced by Megatest in its Megaone test system. Previously, expensive tester resources were shared by a number of pins; per-pin architectures literally put an entire test system behind each pin. As the pin count rises, the cost of test systems rises linearly.

The use of high-speed—and high-priced—ECL drivers and receivers accounts for the high cost of systems employing a per-pin architecture. With its Vista series of logic testers, Tektronix Inc. of Beaverton, Ore., replaces ECL components with CMOS ICs. "We put the edge generation, formatting, and comparison capability for low-speed signals, clock, and pattern data that feed into each tester pin into two CMOS ASICs to make signal routing easy," says Michael J. Kondrat, marketing manager for Tektronix's Semiconductor Test System Division.

Using only two CMOS ASICs trims space and power requirements and boosts reliability, he says. In building pin electronics in CMOS instead of ECL, Tektronix had to solve one major CMOS deficiency: its tendency to drift with temperature changes. The company uses a patented technique, already built into analog circuits for temperature compensation in its spectrum analyzers, for temperature compensation of the CMOS chip, Kondrat says. The solution consists of a temperature feedback loop on each chip to keep the die temperature constant. Although critics say the compensation circuit is a slow-response servo loop, performance data from Tektronix indicates the solution works.

Asix Systems Corp. has taken a different approach to solving the CMOS instability problem. The Fremont, Calif., company has developed a CMOS chip that contains circuits to produce up to six different timing edges and period generators that can produce multiple time sets and be switched on the fly for each pin in the tester. The chip features a circuit that automatically compensates for changes in voltage, temperature, process variation, aging, and other factors, says Richard Bullen, director of marketing at Asix. "The circuit completely eliminates the problem of drift in CMOS," he asserts. The chip contains electronics for two channels; a two-sided board can hold eight chips on a side, a total of 16 channels on a board.

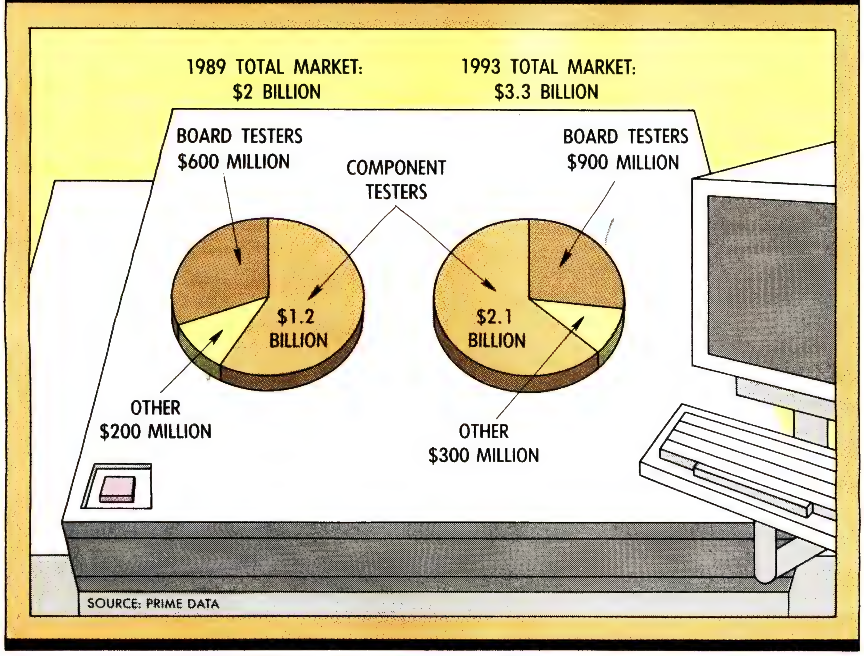
Asix also offers an address-generator chip built in gallium arsenide. The device provides a memory-management system that multiplexes banks of lower-cost DRAM, sending a stimulus to and capturing a response from the device under test. The address generator enables the tester to operate at the same rate as more expensive SRAM-based systems.

The Asix 3 test system, which will implement both of the company's new devices, is slated for release in the first quarter of next year. "The new system will provide the functionality of testers costing up to $3 million or more, but will cost under $1 million," says Bullen. Asix has also announced a merger with Santa Clara, Calif.-based Semiconductor Test Solutions.

Testing now ranks as a big factor in the cost of producing an electronic component, so component ATE vendors are making an all-out effort to lower the costs of their systems

The use of built-in testability or scan circuits has been limited by the real estate penalty—on the order of 12% to 30% of device size—that designers had to pay to put circuits on their devices. With the development of ever denser ASICs, however, designers have no choice but to use scan technology, says Fred Berneche, manager of ASIC test development at Motorola Inc. He says Motorola is implementing scan in its MCA bipolar and HDC CMOS gate-array line. Motorola is not alone in providing scan circuits on its denser ASICs. VLSI Technology Inc. of San Jose offers scan circuits for its line of standard-cell products. This month the company also announced the availability of boundary scan—circuits installed on an ASIC's input/output pins to ease board testing. Other foundries offering scan circuits include LSI Logic, NCR Microelectronics, and NEC.

THE MARKET PICKS UP



SOURCE: PRIME DATA

Motorola has also entered a partnership with the ATE Division of Schlumberger Technologies of San Jose to develop semiconductor test equipment employing built-in scan circuits. David Carpenske, vice president of strategic products at Schlumberger, estimates that current test systems cost about $8,000 to $10,000 per pin.

"Our new test system will cost $1,500 per pin, nearly an order of magnitude difference in price," he says. Schlumberger has already shipped a prototype of the system, code-named Typhoon, to Motorola. Karpenske says the system will be equipped to handle a wide variety of different scan logic circuits.

Makers of conventional component test systems have also begun to beef up support for scan design. Logic Master XL from Integrated Measurement Systems Inc. of Beaverton comes with a scan test module. The module supports the Institute of Electrical and Electronics Engineers' proposed P1149.1 standard for joint test action group (JTAG) boundary scan, scan path, scan set, random-access scan, level-sensitive scan, and other forms of boundary scan. Semiconductor Test Systems offers similar capability in its STS 8500.

The JTAG specification is supported by 200 companies and is actively promoted by Texas Instruments Inc. of Dallas. The specification defines a four- or five-wire test bus that connects the test circuits built onto ICs mounted on a printed-circuit board. A test-access-port (TAP) controller, an IC on the pc board, controls the test bus; it directs the operation of I/O scan cells built into individual ICs or ASICs on the board between the chip's I/O pad and its core.

In normal operation, the cells are out of the flow of data. The scan cells are connected to form a shift register. Each stage in the register is connected to one of the chip's I/O pins. In test mode, the TAP controller serially shifts a stimulus pattern to the scan cells over the test bus. Once the pattern has been loaded, the TAP controller strobes the data into the core of the chip. At the output pins, the resulting response is captured in the output scan cells and then read out by the TAP controller. A board test system supplies stimulus to and reads response from the TAP controller.

TI is building boundary-scan cells into its standard discrete-logic IC families and is providing the TAP controller IC and other ICs needed to implement scan on a board. VLSI Technology is one ASIC supplier that is facilitating the use of JTAG scan in board testing. The company introduced this month a development kit that significantly eases the job of adding JTAG scan cells to ASIC design. The Boundary Scan Kit operates in the VLSI Technology's V8 ASIC Design Platform and contains a test library of 11 cells that can be added to an ASIC design to provide full JTAG P1149.1 support. The kit operates with any of the company's 1.0-, 1.5-, and 2.0-μm gate-array and standard-cell CMOS libraries.

Teradyne's L353 board tester, like the rest of the new L300 series, features a digital command processor that loads scan-test patterns into the pin-electronics RAM.

Makers of board testers are also adding functionality to accommodate the built-in testability that semiconductor vendors are adding to their ICs. Schlumberger's S790 is the first system to offer scan-testing capability on every pin of the system (see p. 81). The L300 series of testers from Teradyne features a digital command processor that loads scan-test patterns from test-system disk memory into the pin-electronics RAM. The patterns are then delivered at high speed to the test pin on the board connected to the TAP controller in a board designed for boundary scan. The tester features a dedicated serial pattern processor to cut the time it takes to load patterns.

Suppliers of board testers are adding more processing power to their systems to perform tests faster. The L300 systems from Teradyne contain fast analog instruments and faster relays for routing analog instruments to individual pins on the board. "The L300 can execute 700 different resistor measurements and up to 250 different capacitor measurements per second," says Larry Klein, engineering manager for the L300. "Before it took 64 seconds to test a complex board, of which 35 seconds were spent on analog circuits. Now, the entire board can be tested in 21 seconds, and only a second is spent testing analog circuits."

In its GR2286 board tester, GenRad Inc. of Concord, Mass., reduces testing costs by applying more power to the problem. Earlier members of the GR228X family used as their central controller the MicroVAX II, rated at 0.9 million instructions per second, from Digital Equipment Corp. of Maynard, Mass. The new system contains the more powerful 2.6-mips MicroVAX III. "The more powerful computer provides almost 30% improvement in test time," says John Lyons, technical marketing manager at GenRad. "The MicroVAX II-based GR2282 tested a pc board containing a 68030 microprocessor, 150 ICs, a number of ASICs, and 8 Mbytes of RAM in 28 seconds. The GR2286 did it in 20 seconds."

Another way to cut test time is to reduce the time spent in mounting and handling the board under test. The L300 features a higher-throughput handler, says Teradyne's Klein. The two-sided surface-mount fixture can handle SMT devices with 25-mil feature sizes and 30-mil pads.

Hewlett-Packard Co. has also developed new handlers that speed the job of mounting and testing a board. Its combinational in-circuit functional tester, the HP3070SMT, comes with a handler that is particularly well suited for probing on boards densely populated with surface-mounted devices. The handler increases probe placement accuracy by a factor of 10. This permits an error rate of 48 parts per million, an order of magnitude better than the 465 PPM other handlers achieve. The system can accommodate up to 2,592 access points on a pc board.

Besides a move to cut test costs on expensive systems by reducing test time, other ATE vendors are developing test systems that are priced under $10,000 and effectively test only certain tpyes of boards. Examples of these include the Model 900 from John Fluke Manufacturing Co. Inc. in Everett, Wash., GenRad's 2275 and 2276 Manufacturing Process Analyzers, and the EMX10 from Summation Inc. of Kirkland, Wash.

The Fluke Model 900 uses reference devices such as ASICs, programmable-array logic, or other types of semicustom VLSI devices to verify the operation of actual devices on a pc board under test. In addition, test systems in this price range use certain techniques to gain control of the board—central-processing-unit or read-only-memory emulation, for example. The system actually tests the board by emulating the board's CPU or the instructions being executed by the CPU.

For example, the Summation EMX10, released last month, uses ROM emulation. The emulator comes with a logic-cell array that can be configured to collect diagnostic information from the board under test. The information can be used to repair a faulty board.

Another approach to low-cost testing is embodied in the GenRad 2275/76 Manufacturing Process Analyzers. The systems use analog instruments to detect digital chips that have been inserted improperly during manufacturing. At under $70,000, these systems are a low-cost alternative to more expensive in-circuit testers. ☐

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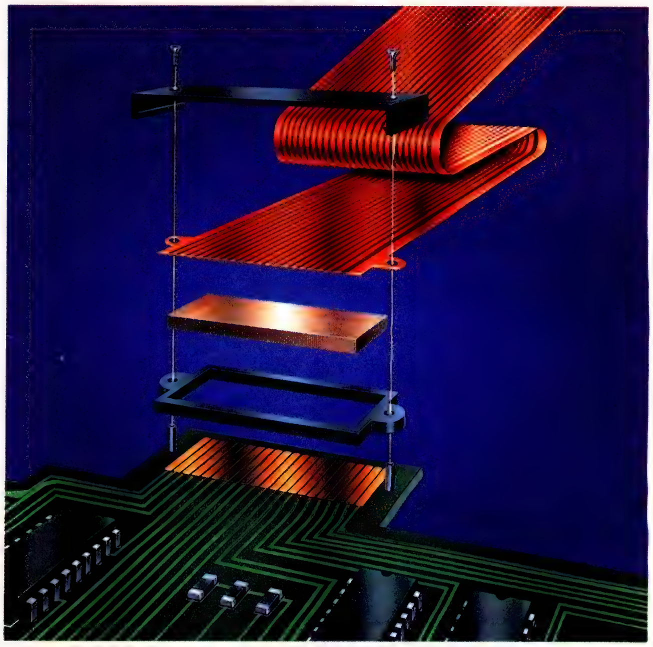

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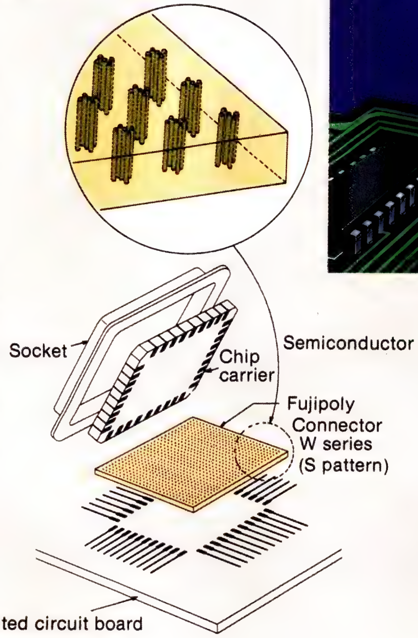

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Circle 111

COMPUTER-AIDED TESTING GETS REAL

BY SAMUEL WEBER

TEST ENGINEERS NOW HAVE ACcess to a universal board tester that offers the kind of power and flexibility that design engineers get from work stations and computer-aided design and engineering tools. The S790 from Schlumberger Technologies implements what the San Jose, Calif., company bills as computer-aided test engineering, or CATE. Housed in a Sun Microsystems Inc. Sun 3 work station, the tester features an open architecture and extensive modularity. It can be custom-tailored to almost any application, Schlumberger says.

Carrying a price tag of $500,000 to $1.2 million depending on configuration, the S790 is aimed at the high end of the board-test market. Here, competition is intense, says Ken Neff, vice president at market researcher Prime Data in San Jose, Calif. This market is dominated by the likes of the GR2750 from GenRad Inc. of Concord, Mass., and the L300 from Teradyne Inc. of Boston. But Schlumberger's advanced software capability will give the S790 the edge it needs to compete successfully, predicts David Brock, the S790 product marketing manager.

The S790 from Schlumberger gives test engineers the same kind of power and flexibility that design engineers enjoy on work stations

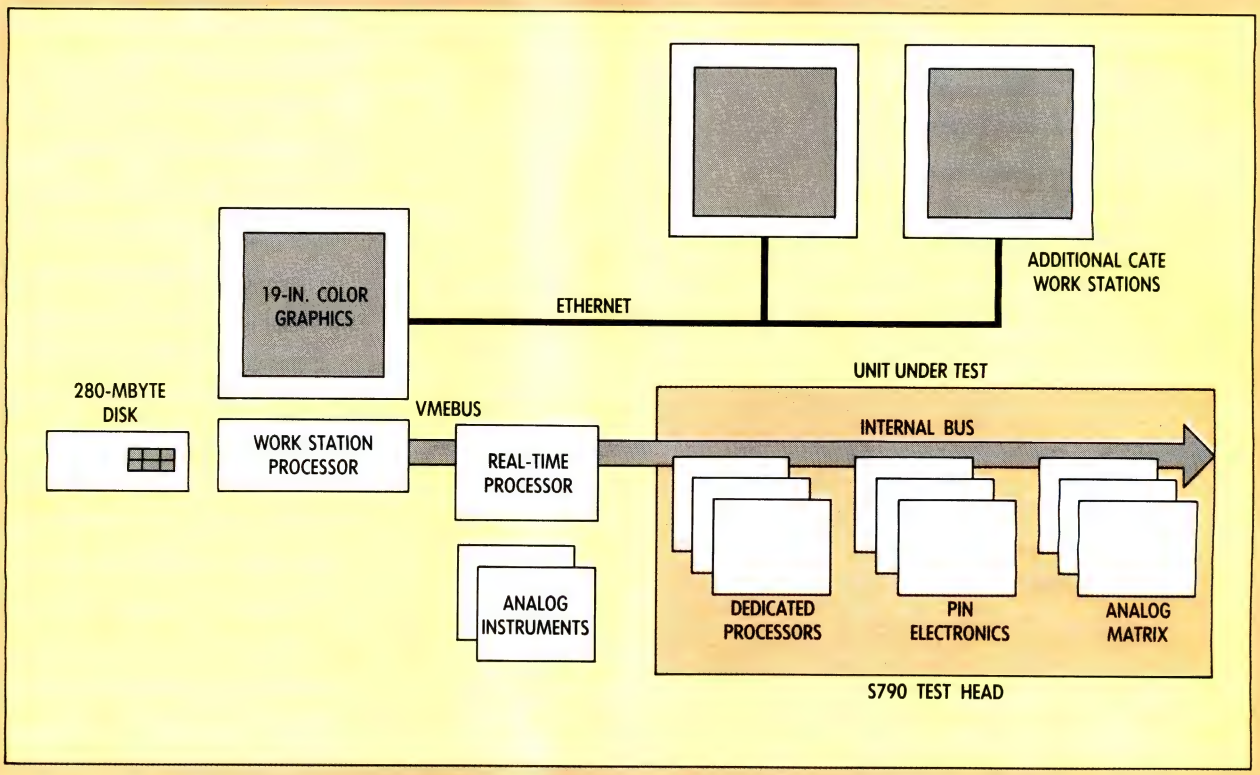
◆

The unit's software, written in C, runs under the Unix operating system. The tester is controlled by PSOS, a real-time operating system. An icon-driven user interface compatible with X-Windows greatly eases the task of developing test programs. Code is transparent to users.

The open architecture allows the S790 to link to simulation data bases, netlists, schematic-capture packages, board-layout files, and other third-party software. Ethernet is used for data-base transfers between CAD/CAE systems, simulators, and the tester's processor. The Electronic Data Interchange Format 2.00 accommodates netlist and schematic data transfers. Gerber file formats are used to transfer board layouts, and CADDIF (Computer-Aided Design Data Interchange Format) provides simulator transfers for cluster or full-board simulations, as well as for device libraries for in-circuit tests.

The S790's Test Plan Strategizer component helps engineers develop a test strategy before writing any code. The Strategizer defines power-supply setups, in-circuit test routines, cluster test routines, and memory, functional, and analog

INTRODUCING: COMPUTER-AIDED TEST ENGINEERING



Hardware architecture for the S790 implements Schlumberger Technologies' concept of computer-aided test-engineering (CATE) work stations. It is designed to facilitate data transfer between design and test.

tests, including "if" and "branch" statements. Each test is represented by an icon that opens up to include the proper virtual instrument, libraries, digital timing, schematics, diagnostic messages, and tools to be used. Links between applications and libraries and their underlying code are automatically maintained.

The Digital Workbench component is a graphical interface that enables users to view digital activity and the relative timing of that activity. It overlays on CAD-DIF and allows vectors to be sent to a fault simulator or the tester bidirectionally. With the Workbench, a user can develop and analyze the digital portion of test programs, defining timing protocols, pin assignments, and modes of operation as well as analyzing test vectors before, during, and after debugging.

The S790 comprises six hardware modules: the Sun 3 work station, a Motorola 68020 microprocessor that serves as the tester controller, universal digital pins, a digital timing subsystem, an analog matrix, and an analog subsystem. The tester's timing facilities allow data stimulus or capture rates from 10 to 40 MHz, depending on the format selected. Timing resolution is 200 ps with an accuracy of ±3 ns.

In the S790's universal-pin configuration, each pin is capable of sinking or sourcing 100 mA or 500 mA, which means that in-circuit, cluster, or performance measurements can be made on any pin. Each pin can have its own drive and receive voltage levels for different logic families or for testing voltage margins. Selectable slew rates enable the tester to accommodate various logic families with different rise and fall times. Each pin also has a corresponding analog "highway," allowing in-circuit tests of analog components using three-, four-, or six-wire measurements for analog or hybrid printed-circuit boards.

The S790 also deploys a proprietary pin-multiplexing scheme called Flexpin, says Brock. Flexpin is the only multiplexing architecture for automatic test equipment that allows all the remaining pins to be latched either high or low while the "true" pin is connected to one of the multiplexed pins. This design eliminates fixture and pin-contention problems and allows fixture configurations to be changed via software.

The S790 provides 32 universal test channels per module, for up to 960 pins; 32 high-voltage test channels per module, for up to 960 pins; and 16 or 128 Flexpin test channels per module, for up to 3,840 pins. The analog matrix supports up to 28 virtual instruments. A 30-MHz module accommodates up to 512 pins; a 5-MHz module handles up to 1,024 pins.

According to Brock, another feature that gives the system its powerful capabilities is Analyst, a fault-isolation algorithm based on artificial-intelligence techniques. The Series 700 Analyst software included with the S790 controls the tester's diagnostics facilities.

After Analyst locates a problem mechanism or component, the data can be transferred to Tactician, a management tool for improving productivity and quality in a manufacturing environment. Tactician simplifies the test-repair interface and identifies process problems rapidly. Test and repair data are collected on line and incorporated automatically into the Tactician data base. With Tactician, board-repair information is logged, and the data is analyzed and used to generate reports on yield and productivity trends.

"Our aim is to supply software and hardware that reduce diagnostic program generation time and to make it easy to find out what is wrong so the user can do something about it," says Brock. "We think we have the most advanced diagnostic user-proof software available." ☐

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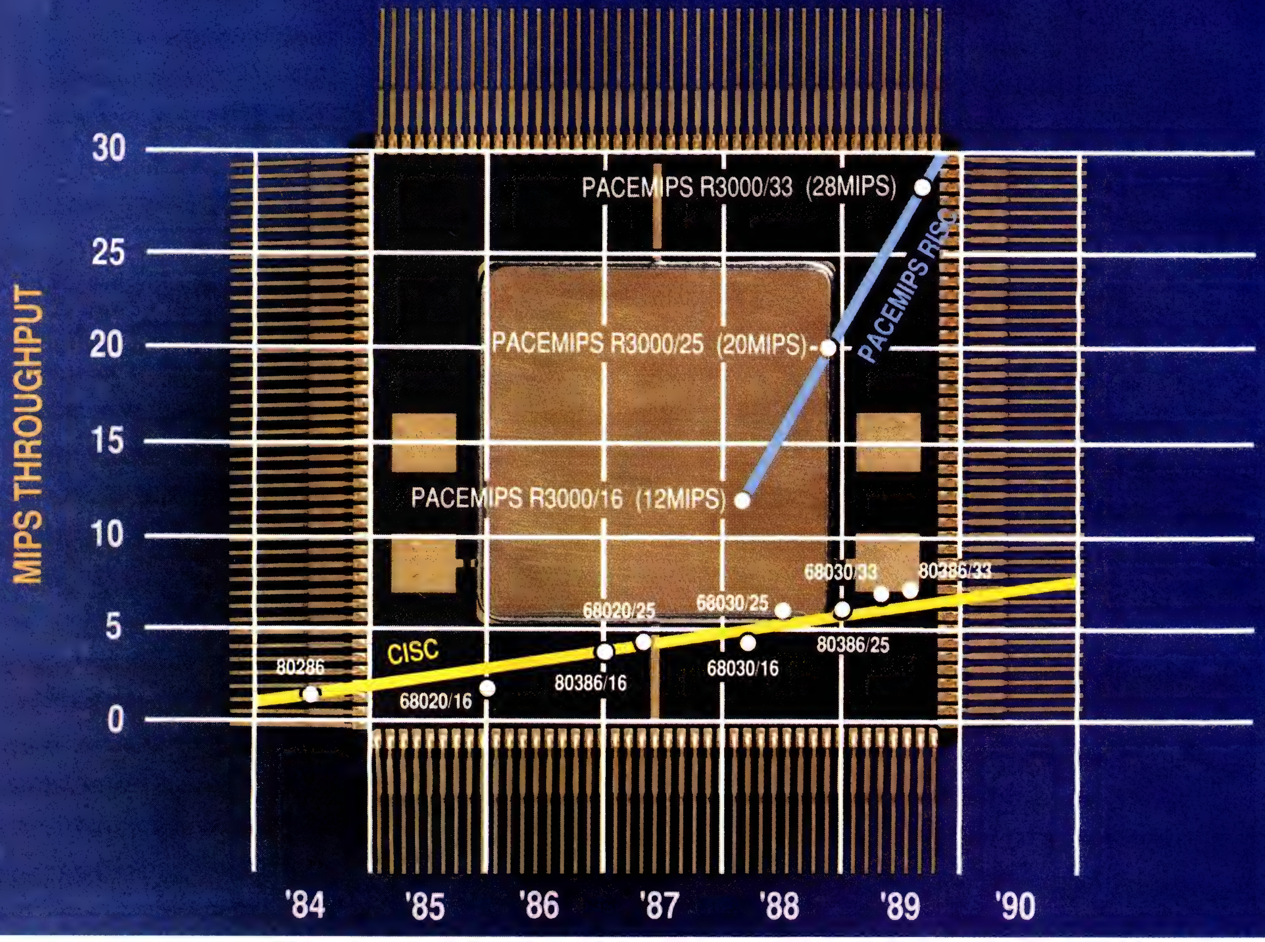

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SCALABLE SYSTEM CONCEPT HITS ATE

ONE MAKER OF AUTOMATIC test equipment is now riding the trend toward scalable architectures that is driving the minisupercomputer market. Teradyne Inc. has announced a scalable and user-configurable advanced linear device tester that not only offers high performance but also can be easily expanded to accommodate future improvements in linear-device performance.

> **Teradyne's A510AL linear-IC tester provides three levels of configurability—and it can be expanded to accommodate devices of the future**
>
> ◆

Teradyne's A510AL, the newest member of the Boston-based company's A500 family of ATE offerings, is designed to test advanced linear integrated circuits ranging from high-speed operational amplifiers to linear arrays and user-specific ICs.

The A510AL's scalable architecture lets users tailor the system—via hardware and software—to handle the most demanding linear ICs without limiting the ability to add instrumentation later for devices still on the drawing boards.

Test systems for advanced linear ICs must be sophisticated enough to enable a device vendor to guarantee on data sheets specifications that either haven't been measured before or were reported only as "typical" numbers. For example, if testing gear for high-speed op amps can't measure settling time less than 200 ns, a vendor may list 200 ns as the typical settling time even if its products are faster. Michael Luttati, product manager for the A510AL, says the test system can measure settling times below 20 ns, allowing an IC vendor to differentiate its products from the competition.

The A510AL sports many of the A500's advanced features, including dual Sun Microsystems Inc. computers, the Unix operating system, C-based Interactive Menu-Assisted Graphics Environment (Image) software, and Ethernet networking. The original A500 tests mixed analog and digital VLSI devices; the A510AL tests high-performance linear ICs, a category that includes low-noise op amps, high-speed comparators, precision references, precision automotive devices, and application-specific ICs.

Teradyne says its A510AL offers users a highly flexible architecture that can be customized by mixing and matching mainframe and

BY LAWRENCE CURRAN

test-head instruments via the Image software to establish an optimum signal-delivery path to and from the device under test. The three-tiered Grid architecture lets users configure the signal path to and from the device under test at each level instead of having to rely on the fixed signal paths used in conventional test systems, according to the company.

At the top level lies a configuration board, which routes signals from the test-head modules to the device under test. Luttati describes this as a multilayer board that also carries the wires that connect to a device-interface board. Teradyne is offering a series of configuration boards from which customers can select one or more appropriate units.

Below the configuration board is the test head itself; most of its modules are custom-configurable and can be dependent on or independent of the test system's mainframe instruments. These general-purpose slots permit a user to add new modules that integrate into the system's architecture. "If a year from now we want to add an instrument to test frequencies of 1 GHz instead of 500 MHz, we can do it easily," says Marc Levine, a Teradyne engineering manager.

This highly flexible architecture is easy to customize: users simply mix and match mainframe and test-head instruments by means of the Image software

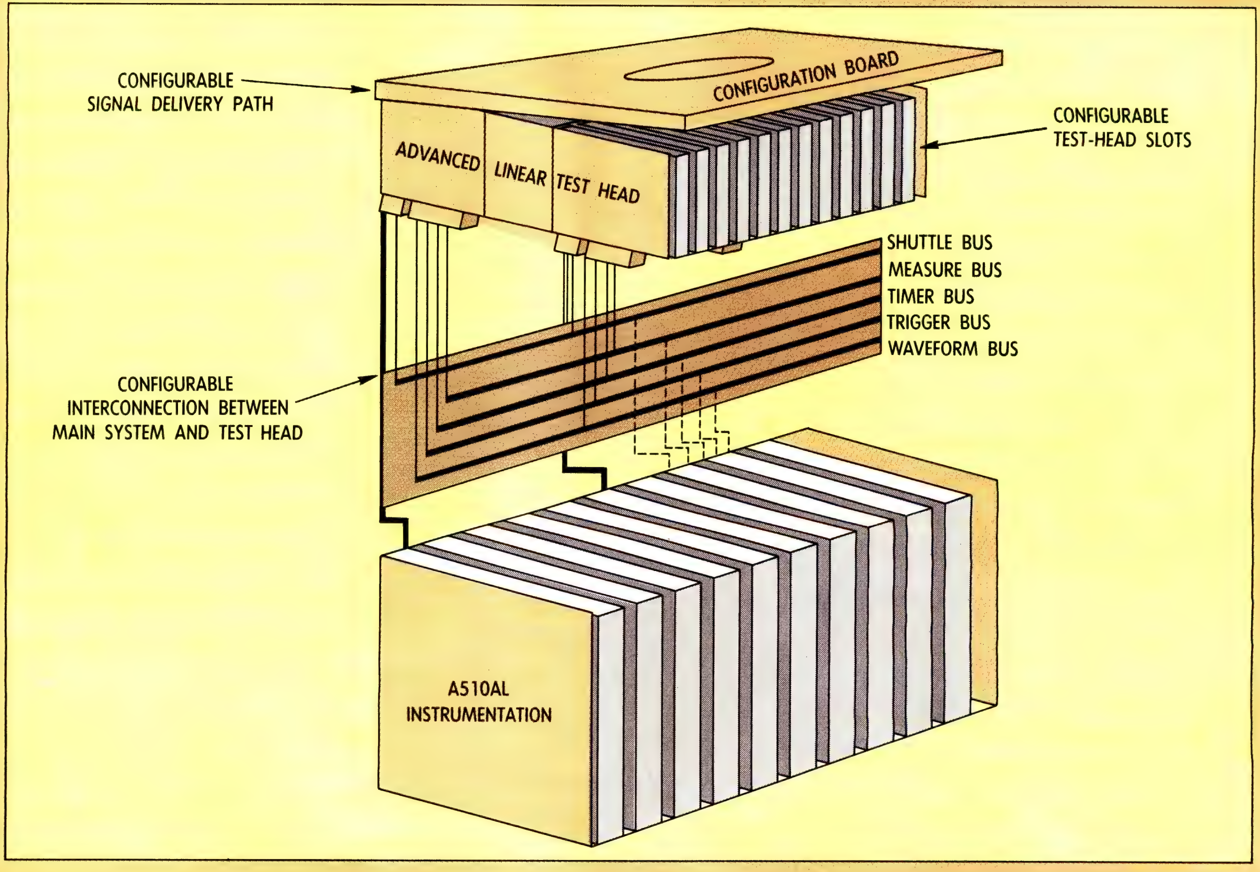
Signals travel among the A510AL's mainframe instrumentation and the test-head and configuration board over a set of user-configurable buses. These analog and digital buses include a shuttle, measure, timer, trigger, and waveform bus, each of which enables bidirectional signal distribution between the mainframe instruments and test-head modules for synchronization and signal processing. Customers can route any of those signals interchangeably along any of the buses to or from any instrument in the mainframe or channel card in the test head.

"We're offering three levels of configurability instead of the usual fixed interface to a device under test," says Michael Bradley, product marketing manager at Teradyne. "The fixed interface reflects a short-sighted strategy that assumes the market won't change substantially."

Luttati asserts that 75% of the channel cards in the test heads of conventional testers are usually fixed—dedicated to provide a given signal, such as a radio frequency or high-power stimulus. In contrast, 75% of the A510AL's test-head channel cards are user configurable, and only 25% are dedicated.

The A510AL is scheduled to start shipping in the first quarter of next year. Prices for typical configurations will range from $375,000 to $650,000. ☐

CONFIGURABILITY ON THREE LEVELS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A510AL INSTRUMENTATION

Customers can configure Teradyne's A510AL advanced linear test system at three levels of its architecture. Slots in the test head let users add new modules for testing next-generation devices.

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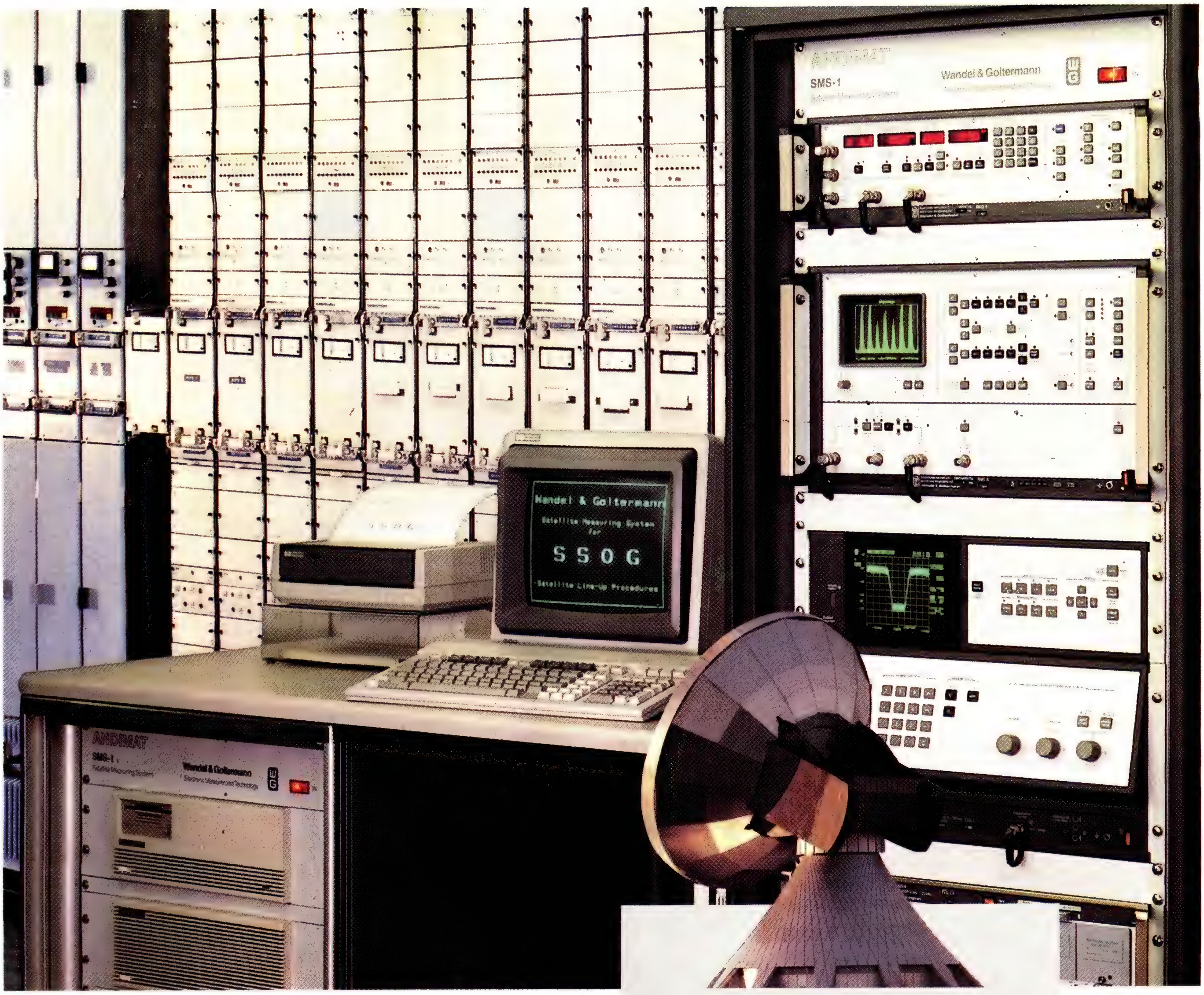

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VOICE PROCESSING REACHES OUT TO TOUCH EVERYONE

BY JACK SHANDLE

The days of simple voice-mail messages are numbered. A technology spurt keyed on digital telephony data streams, coupled with competition among phone-network service vendors, is sparking a new wave of sophisticated voice-processing systems. The momentum is sure to build, making new market opportunities for system integrators, original-equipment manufacturers, and software developers. Greasing the skids is a movement toward a common specification that lets dissimilar machines exchange messages and a universal terminal that can handle many data formats.

> ***The industry is on the brink of adopting a voice-processing specification that will let multivendor systems communicate***

With network-service providers such as AT&T, MCI, and US Sprint opening their networks to outsiders, voice-processing companies can access the intelligence residing in the network and leverage products on it. Caller identification presents a major opportunity in this area—no longer will customers have to repeat the same information every time their call is transferred. And the trend from analog to digital signaling makes the integration of other data types—such as facsimile and electronic mail—into a voice format just a matter of time.

Besides invading the once sacred turf of the network operators, voice processing is also infiltrating the computer world. "There is increasing integration into existing data bases," says Dave Ladd, executive vice president for product development at VMX Inc. of San Jose, Calif. "The key is to provide software tools that make the design of applications easier to accomplish. That is, to design solutions for groups of customers or individual customers."

Businesses such as catalog sales, financial services, insurance, and trucking are among early adapters of the new wave of voice-processing technologies. But the most glamorous of the new technologies—speech recognition—is still "one or two years away," says Ladd, even in its most rudimentary applications.

Besides VMX, major players in the voice-processing arena include AT&T, Boston Technology, Centigram, Digital Sound, Genesis, Harris, Octel, Rolm/IBM, Voicetek, and Wang Laboratories.

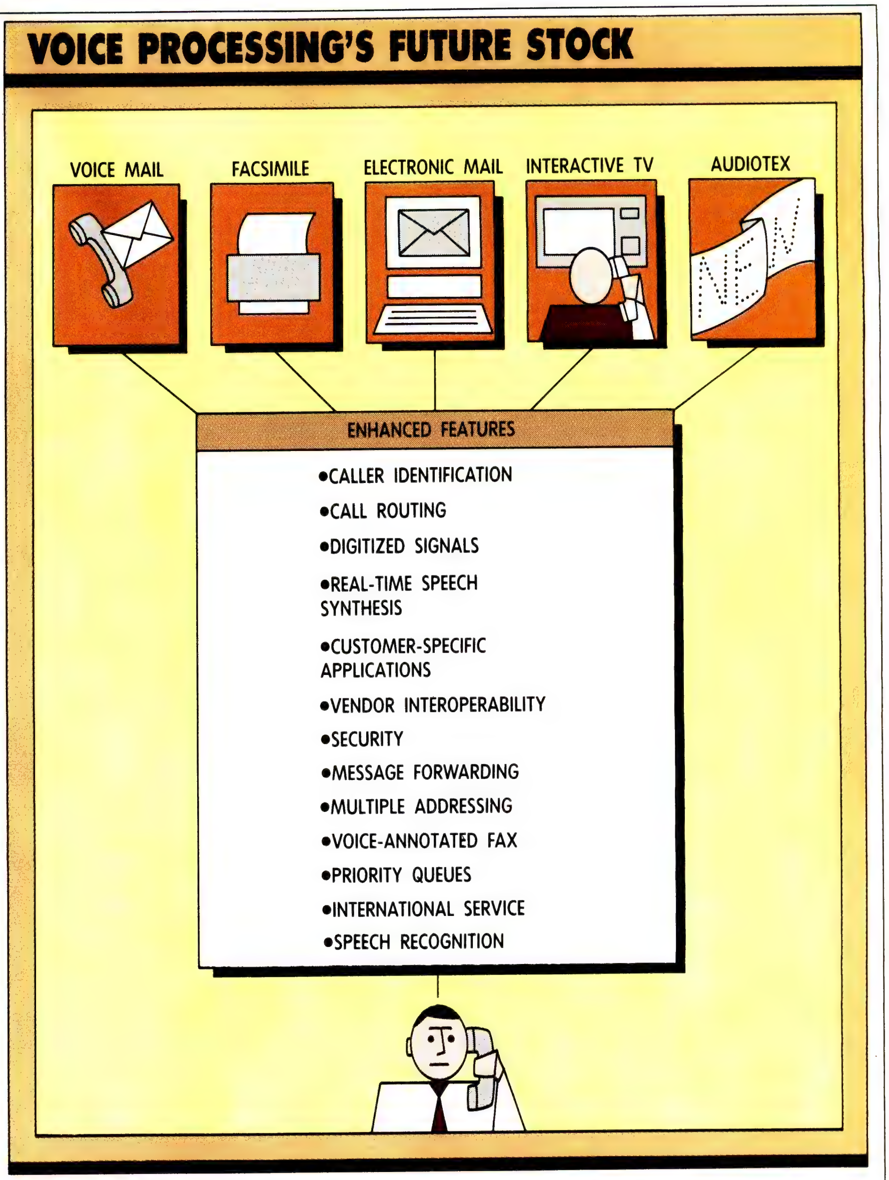
Long a technology in which proprietary systems reigned supreme, voice processing took its first step toward a universal specification a year ago, says Bob Mercer, senior vice president of Hatfield Associates Inc., the Boulder Colo.-based consultant spearheading the standards drive. That's when the 35 companies involved in the movement decided not to initially take the tortuous route of developing a standard under the auspices of an official body, such as the American National Standards Institute. Since then, the group—which includes vendors and large users alike—has moved quickly.

The result is the Audio Messaging Interchange Specification, or AMIS, which is slated to be completed in a meeting this month. A few vendors are already talking about taking the specification to a standards body, says Mercer.

The AMIS community will probably end up with two versions of the specification. "One will be a full-blown spec based on digitally encoded signals with a structured data format and message flow," Mercer says. "The other will be a simpler analog protocol where signaling will be done in the dual-tone, multiple-frequency mode. Messages will be transferred as a regular voice message."

The protocol will mandate relatively few basic features for machine-to-machine communication. These involve ways for dissimilar systems to send, receive, reply, and forward messages to one another. Reply means the receiving machine will be able to send some messages—such as simple received-message acknowledgments—without human intervention. Message forwarding means automated redirection of the message to another electronic mailbox.

Several advanced features are not mandated, says Mercer, but a few are. Most notable among these is a protocol for notifying the sending machine that the receiving machine is incapable of performing a requested task. Some of the other advanced features include privacy and security implementations, and distribution lists that make it easy to send the same message to multiple addresses without separately addressing each one.



With the phone keypad working as a computer terminal, voice-processing technology will soon encompass a range of media: fax, e-mail, even interactive TV.

Just as important as AMIS's feature set are the attributes it mandates. These include minima and maxima limitations, such as the maximum number of addresses allowable for a message; a time stamp for each message; priority/send and priority/receive codes for queued messages; and a code at the receiving machine indicating message importance. The AMIS committee's decision to develop both analog and digital protocols represents a balance between past and future technologies, says Mercer. The analog protocol addresses the great bulk of voice-processing systems in use today. The richer, more robust digital protocol anticipates the arrival of the integrated services digital network and, in the more immediate future, an evolution toward digital signals in telephony.

A technology leader in the digital processing of voice messages is Boston Technology Inc. Thanks to a trail-blazing standard platform, the two-year-old Cambridge, Mass., company saw its market share grow from virtually zero to about 3% in 1989. Its revenues grew to $25 million this year from $2.5 million in 1988, says chairman and chief scientist Scott Jones.

"We have a tightly coupled distributed architecture that allows us to store information once and access it from any point on a network of units," he says. More conventional systems increase the number of lines served by cascading modular voice-processing units. But in this approach, analog technology presents an access problem: a single message must be stored in each module that might have to access it. Boston Technology's innovation is a digital switch positioned in front of the voice-processing units. With the switch, the company's CO Access system can also be easily scaled up to more lines—a key advantage for the telephone companies that have adopted the product for use in the central offices, says Jones. In the past, most successful voice-messaging companies have concentrated on putting their equipment on the customer's premises, using it in tandem with a private-branch exchange.

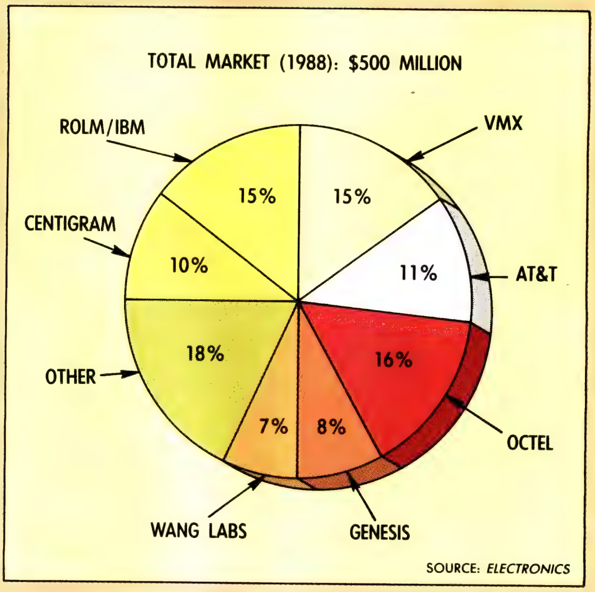
Jones's vision of the technology's future keys upon a versatile platform. "We're in the process now of building a universal platform that sits inside the phone company's office and does considerably more than voice messaging," he says. One feature of the platform will be what the industry calls "audiotex"—the ability to provide information about everyday topics such as weather, sports, and TV or movie listings. Connection to data bases for industries—such as airlines, for reservations and information, and trucking, for dispatch and routing—are narrower variations on the same theme. To follow will be speech synthesis, facsimile store-and-forward functions, and automated attendant capabilities.

But perhaps the most intriguing feature of the phone-based universal terminal is entertainment. "Trivia games can be played by phone," says Jones, "and TV viewers can be linked interactively to game shows by dialing 900 numbers. You need a huge platform to handle all those calls."

In order for a universal platform to reach its full potential, third-party vendors and components manufacturers will need to develop enabling technologies and enhance existing ones.

The most important of these, says Jones, are digitized speech, speech synthesis, speech recognition, and speech verification. "If bank-by-phone is going to become pervasive," he says, "the 10-digit access code will have to be replaced by voice authentication." Digital signal processors can be adapted to create and characterize the spectragram of a particular voice message to see if it matches one already authenticated.

LOTS OF CONTENDERS



SOURCE: *ELECTRONICS*

Combining telephone networks with data bases has become a full-time business for Harris Corp.'s Digital Telephone Systems Division, says director of marketing Ron Derechailo. The Novato, Calif., company's VoiceFrame system capitalizes on the added intelligence that companies such as AT&T, MCI, and Sprint have been allowing customers. In particular, the recently released caller-identification capability lets VoiceFrame identify incoming callers and search a corporate data base for information about them. With this information, it can route the call to the appropriate department or district office, and it can also assign a priority to the caller for processing through a decision tree.

The biggest opportunities for third-party vendors lie in software. "Once the hardware comes together," says Derechailo, "system integrators and software developers that are already in a niche market—such as insurance or automotive-parts supply—will only have to adapt their products to telephone technology."

Real-time processing is another idea whose time has come in this realm. One early implementor—VoxLink Corp. of Nashville, Tenn.—has added the twist of converting electronic mail messages in ASCII text directly to voice. "Up until now," says VoxLink president Bill Brennan, "technology has not allowed us to interpret voice mail and electronic mail, but the combination of improved algorithms and microprocessor technology has changed that."

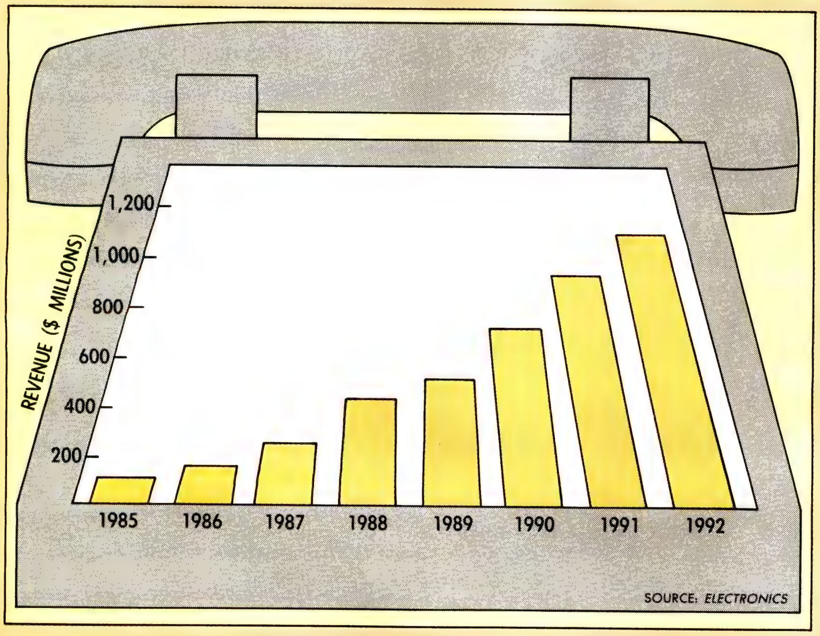
The algorithm reduces ASCII text into phonemes and diaphonemes—the basic elements of speech—using filters and rule-based techniques. VoxLink licenses the algorithm from Speech Plus Corp. of Sunnyvale, Calif. Speech Plus also licenses microcode to IBM, Olivetti, Texas Instruments, and Wang. It uses Intel Corp.'s 80186 microprocessor teamed with a DSP to execute it in real time. "Although there are always exceptions in actual speech to the rules we use," says Brennan, "the human brain adapts quickly using the context of the sentence."

Other products, including IBM/Rolm Corp.'s recently introduced Call Path, have similar capabilities. "In the future, we want to seamlessly integrate applications as you go from one to the next," says Charles Jollisaint, chief architect for the Santa Clara, Calif., company's product. Voice-annotated facsimile would be one example.

Speech recognition presents the most exciting prospect for turning a telephone into a computer terminal, but it is also the technology that is furthest in the future. AT&T Microelectronics Inc. of Berkeley Heights, N. J., has a speech-recognition chip ready for unveiling by the beginning of next year, but its target market will be cellular phones for cars. After programming by the car's primary phone user, the chip will recognize enunciated names, cross-reference them to a directory, and dial automatically with no need for the driver to let go of the wheel.

"Right now, voice recognition is not quite cost-effective enough for generalized deployment," says Jollisaint. Security stands as one application where the technology would be cost-effective, he says, because of the resources at risk. "Transactions with a stockbroker would be an example," he says, "as opposed to it just being a user-friendly aspect of a voice-processing system." ☐

DIALING BIG REVENUES



SOURCE: *ELECTRONICS*

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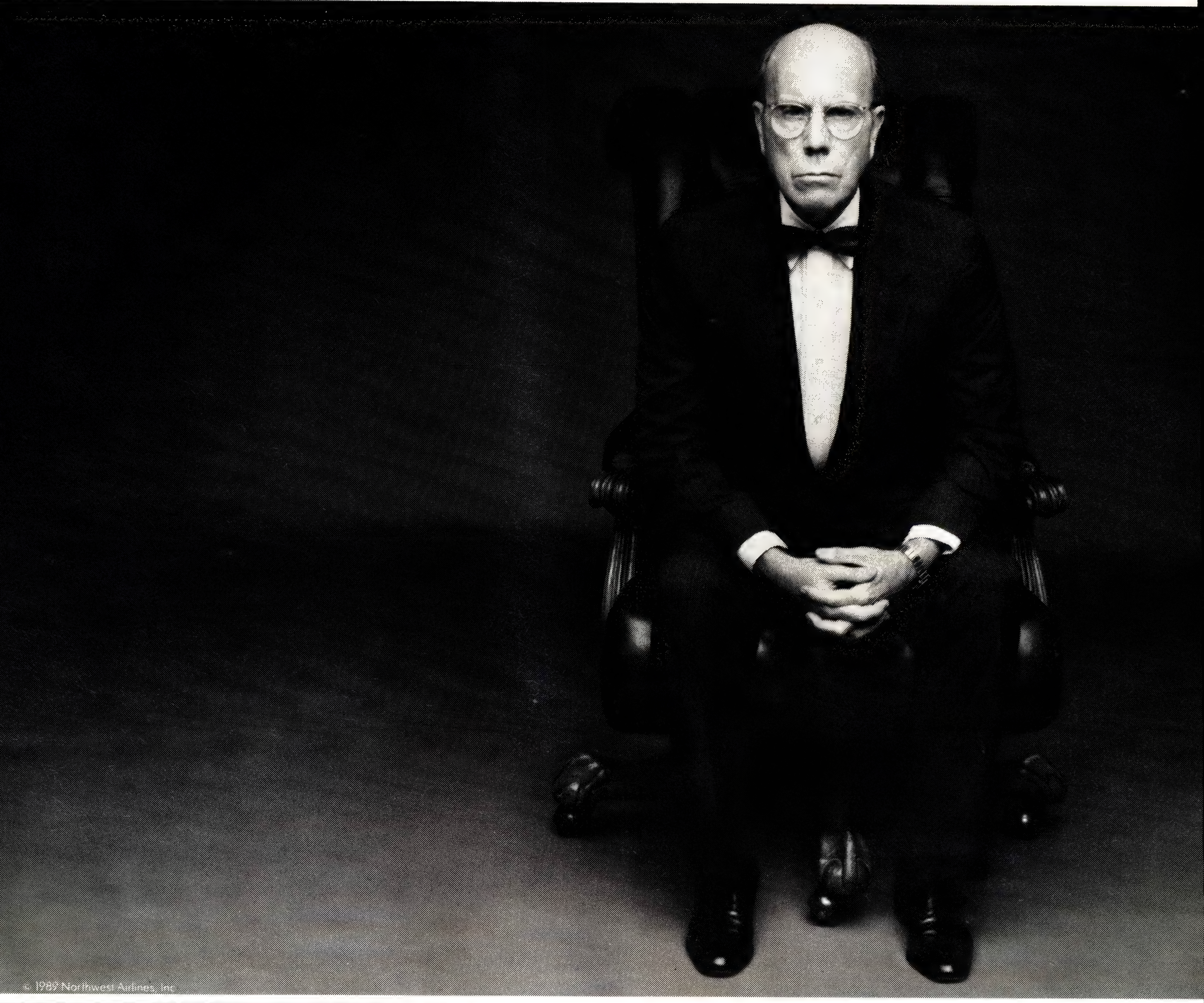

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NORTHWEST AIRLINES

MAKE ROOM FOR POCKET COMPUTERS

Battery-powered models are the fastest-growing segment in the business—and the 1-lb machines are the talk of the show at Comdex

Atari's Portfolio is the tiniest portable computer yet: the 1-lb unit is slightly smaller than a standard video cassette tape. It costs $400.

Move over desktops, move over portables, notebooks, and laptops. Make room for a new class of personal computer that will hit the floor at this month's Comdex/Fall '89 Exposition in Las Vegas. Variously referred to as handheld, palmtop, or pocket computers, the new machines cram the functions of a laptop, or even a desktop, into the smallest, most personal portable yet—a flat, notebook-size affair of around a pound that slips into pocket or purse.

Coupled to the introduction of several compact and high-capacity data-storage peripherals, this means that those catchwords of electronics—smaller, faster, denser, cheaper—will apply once again to the annual conference for computer distributors running this year from November 13 through 17. More than 1,700 exhibitors from around the world will display their wares at the Las Vegas Convention Center and nine hotels in the area. Attendance at the gathering is expected to top 110,000.

Portable battery-powered computers represent perhaps the fastest-growing segment of the computer industry. Last year about 820,000 of the 10 million MS-DOS computers sold worldwide were portables, says market researcher Dataquest Inc. of San Jose, Calif. This will climb to 1.2 million units this year and pass 3.5 million units in 1993.

Technology is fueling this growth because of what Atari Computer marketing manager James Fisher calls "America's constant quest for portability." The more than 30 million desktop PCs used by business today are the targets for portable systems, says Stav Prodromou, Poqet Computer Corp.'s president and chief executive officer. "Business people and professionals no longer have to leave information in their computers in the office," Prodromou says. "They can take

BY ALFRED ROSENBLATT

their essential files and programs to a meeting down the hall or anywhere around the world with none of the limitations imposed by the bulkiness and short battery life of other portable computers."

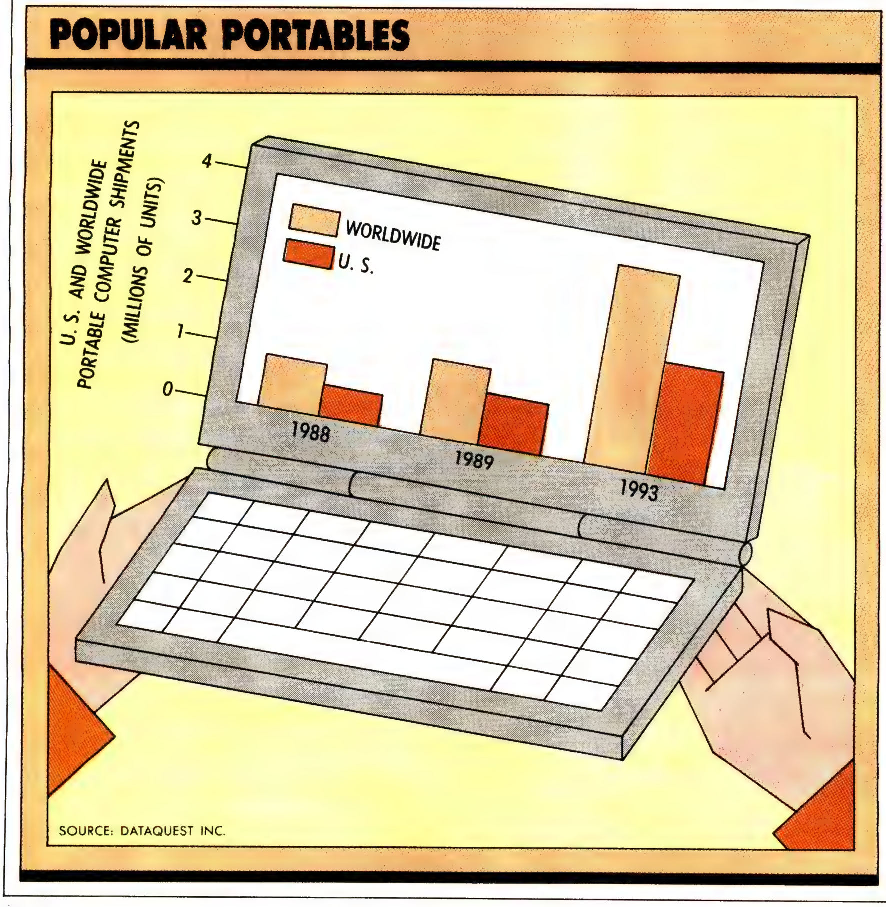
In addition, commercial applications are being found for the small computers that never existed before, especially by salespeople who travel to the premises of their customers. Via the computer, all manner of product information can be accessed, either from computer storage or from the home office. Via the display, customers can also be shown how different alternatives to a custom design, such as cabinetry or closets, might look.

But if there is no desire for portability in its own right, there may be a desire for freeing the top of one's desk from the PC. Two Sunnyvale, Calif., companies are betting that executives with desktop PCs will scale down even beyond portables and laptops. The Poqet PC from Poqet (pronounced "pocket") Computer and the "palmtop" Portfolio from Atari are the smallest PCs yet to surface, though other companies may bring their versions to Comdex, as well.

The new pocket PCs have certain features in common. They do without floppy-disk drives (indeed, the absence of rotating drives is one way to classify the smallest of computers). Instead, the computers rely on card drives and solid-state credit-card-size memory to store programs and data. These cards come with random-access memory, programmable read-only memory, or masked ROM. Their designers have also done everything possible to cut down on the machines' power consumption. They use a CMOS microprocessor like the 80C88, components like CMOS RAM, and a liquid-crystal display. Elaborate power-management features have also been developed.

Not only do the notebook-size machines make data more portable even as they ease desktop clutter, but new commercial applications are being found

For example, while the machine waits for a user to type, Atari's Portfolio automatically switches into a standby mode. This mode, which actually stops the microprocessor clock, is transparent to the user because the screen does not go blank and there is no delay when work is resumed. The system also turns off automatically if no entry has been made for two to four minutes.



SOURCE: DATAQUEST INC.

To achieve their compact size, the new machines rely on application-specific integrated circuits to combine functions that would otherwise require multiple chips. And they make heavy use of surface-mount components on two-sided circuit boards. The new computers also come with some kind of built-in MS-DOS operating system and with software such as a Lotus 1-2-3 spreadsheet, word processor, and calculator. There is also file-transfer software to upload and download files to or from a compatible PC. In addition, low-cost options are available, like Atari's $79.95 parallel interface for printers and PC file transfer, its $49.95 serial interface for desktop computers and modems, and memory expanders.

Other options in the works will make the pocket machines even more like desktops. For example, disk-drive makers are working hard to develop very low-powered hard-disk drives with 20 or 40 Mbytes of storage that could even be mounted internally.

The Poqet PC, available this fall for $1,995, offers capabilities parallelling an XT-type compatible. Measuring 8.75 in. long by 4.3 in. deep and 0.9 in. thick, it runs for up to 100 hours on two standard AA alkaline batteries. It operates like a fully functional MS-DOS desktop machine, the company says.

The computer comes with a full 80-character-by-25-line black-on-silver reflective LCD and a 77-key, typewriter-style keyboard. System ROM stores Microsoft DOS Version 3.3, GW Basic, proprietary BIOS, and five application programs. Resolution of the 8-in. diagonal display is 640 by 200 pixels.

Poqet's file-transfer utility relies on Virtual Network Architecture for moving files over a direct cable connection at up to 115,200 baud. Or it can move data via modem at 19,200 bits/s through the serial RS-232-C port of desktop machines.

The 80C88 runs at up to 7 MHz. System memory includes 512 Kbytes of RAM and 640 Kbytes of ROM. Mass memory for file storage and applications depends on two card slots that accommodate 68-pin RAM or ROM memory cards. Current RAM card storage reaches 512 Kbytes, but it's expected to top 2 Mbytes during 1990. Data in the card is maintained by a battery when the computer is off.

Poqet also offers, for $395, a 3.5-in., 1.44-Mbyte floppy-disk drive that runs on four AA battteries. Thus, files and programs can be transferred to and from the hand-held machine on disks compatible with desktop computers. Also, publishers of at least 12 applications, including the Lotus 1-2-3 spreadsheet and WordPerfect Executive, plan to provide software in the ROM-card format for the pocket computer, Poqet says.

Poqet Computer's Poqet PC (top) offers much of the capability of an XT-type machine and weighs only a pound. Grid Systems' GridPad portable accepts hand lettering on a 10-in.-diagonal LCD.

Like the Poqet PC, Atari Computer's Portfolio also tries to provide a look and feel familiar to users of IBM Corp. PCs or compatibles. At only $399.95, however, it may not do everything the Poqet machine can. The 4.92-MHz system runs for 40 to 60 hours on three, rather than two, AA alkaline batteries, and includes an operating system very much like MS-DOS 2.1. However, the operating system must be adapted to things like the Portfolio's 40-column-by-8-line display and 240-by-64-pixel graphics.

Other features include a smaller 63-key keyboard and 128 Kbytes of RAM, expandable to 640 Kbytes. A 60-pin bus connector is used for proprietary peripherals.

A new approach to data entry comes from Grid Systems Corp. of Fremont, Calif., which has extended its desktop computer and battery-powered laptop expertise to develop GridPad, a portable IBM PC-compatible computer that recognizes hand-printed material. The 4.5-lb machine—which has a 10-in.-diagonal, 640-by-400-pixel LCD—is designed for workers who typically gather data and record it on paper forms. Among them: census takers, airline personnel, route delivery drivers, and claims adjusters. People who enter data on forms by hand constitute the largest data-entry application, and it is largely unautomated in the field, says Tim Bajarin of Creative Strategies, a market researcher in Santa Clara, Calif. He sees the GridPad, priced under $3,000, as the "first true portable computer to offer handwriting recognition."

The machine measures 9.25 by 12.4 in., about the size of a clipboard, and it's 1.4 in. thick. Data is entered with an electronic pen applied to the screen. Standard business forms can be displayed on the screen and filled out with the pen. The unit can also capture and store signatures and graphics. Graphics and text are stored as MS-DOS files which can be transmitted by a built-in modem or by facsimile. The computer is built around a 10-MHz 80C86 microprocessor. MS-DOS 3.3 is included in an internal ROM and the machine comes with 1 Mbyte of system RAM. The LCD is CGA compatible.

As with the pocket computers, this one has a power-management scheme; the unit can be switched to a low-power standby mode when data is not being entered. Power for eight hours of operation comes from a rechargeable nickel-cadmium battery, and it can also be operated with an external AC power source or AA alkaline batteries.

A pair of card slots accommodate removable 256- or 512-Kbyte battery-backed RAM cards. A 3-lb stand-alone 20-Mbyte hard disk is available as an option. A 9-pin RS-232-C serial port permits GridPad to be used with peripheral input devices such as bar-code sanners, an important feature in consumer goods distribution and survey applications.

Data can also be entered into the unit on a standard keyboard via an XT-compatible external keyboard port. Thus, back at the home office, the computer can be turned into a desktop machine. It can send and receive electronic mail and data files over a proprietary wide-area network. What's more, alphanumeric characters can be entered via a graphic representation of a keyboard displayed on the GridPad's screen.

Grid Systems is recruiting a variety of software developers to write software for GridPad. It offers a set of development tools in the C programming language to take advantage of the pen-based method of data entry. The company also licenses an applications software-developers tool kit for writing custom forms-based applications and user interfaces.

"Desktop-system replacement" is the raison d'être for the T3200SX from Toshiba America's Computer Systems Division in Irvine, Calif. The 17-lb, $6,229 unit is quite powerful. Built around the 32-bit processing of a 16-MHz 80386SX microprocessor, it has a 13-Mbyte memory capacity, VGA graphics, and operating system support for MS-DOS and OS/2. It measures 14.6 by 15.6 by 3.9 in.

Optical storage is being brought to the battery-powered laptop computer for the first time in a compact-disk ROM drive. The model MXV-101 CD-ROM is just one example of the small but high-capacity storage peripherals being shown at Comdex. The drive was developed by the Northern Virginia Systems Group of Magnavox Electronic Systems Co. Grid Systems is the first to ship one. It is to be used with the company's GridCASE 1500-series laptop computer.

Weighing less than 5 lbs, the unit retrieves up to 550 Mbytes of data. This can be from mass archival documents such as field-service maintenance and reference manuals; it stores the equivalent of 275,000 double-spaced typewritten pages. The CD-ROM has a 5.25-in., half-height form factor and a Small Computer System Interface. A kit that includes a SCSI adapter cartridge and software driver is $1,900, with quantity pricing available. They're manufactured by the Northern Virginia Systems Group in Ashburn, Va.

As for the other new data-storage devices, new highs in capacity are being reached in several different types of units by a range of companies. If the new pocket computers weigh around a pound, how much can a companion disk drive weigh if a computer-toting executive is not to feel loaded down?

Areal Technology of San Jose believes 4.8 ounces to be right. This is the weight of its new microDRIVE MD-2050 hard-disk drive—a 2.5-in. single-platter drive that stores 49.2 Mbytes of formatted data. The drive also meets the 17-mm (0.669 in.) height that makers of the smaller computers are adopting. Its other dimensions are 2.8 by 4.0 in.

In effect, this drive and other 3.5-in.

drives Areal has developed bring the large-scale data storage found in desktop systems to laptops and pocket computers.

Key to achieving the large capacity in so small a size is the disk substrate. It's made of glass, rather than the conventional aluminum. The glass is much smoother than aluminum, which means that the thin magnetic film sputtered on the glass is much smoother too, points out Mike Kirby, Areal's vice president of marketing and sales. This allows the heads to fly very close to the media—about 4 μin. instead of the usual 8 to 12.

This, in turn, leads to higher magnetic resolution and bit densities. The 100 million bits/in.^{2}, twice the density usually obtained, are formatted into over 30,000 bytes/track and 819 cylinders. Average access time is under 29 ms and a transfer rate of 7.5 Mbits/s can be sustained. The drive operates from a single 5-V source and sells for $595 each in volume.

Proprietary spindle and actuator motors, together with the drive electronics, consume only 950 mW—less than any disk drive on the market today, according to Areal. The company says the drive can operate continuously in battery-based systems; there is no sleep mode when data is not being accessed. Initial deliveries are to begin late in the first quarter of next year. A 100-Mbyte unit is due late in the second quarter, with other versions to be announced over the next 12 months. Larger-capacity 3.5-in. drives are also in development.

Aiming at the high-end PC and low-end Unix work station markets, Quantum Corp. of Redwood City, Calif., is adding significantly to the capacity of its ProDrive family of 3.5-in. disk drives. It is displaying six new products with formatted capacities of 120, 168, or 210 Mbytes with either embedded SCSI or AT-Bus controllers. The ProDrive series now has 11 disk-drive products with formatted capacities ranging from 42 to 210 Mbytes.

Three of the new drives offer the industry's first implementation of the recently introduced SCSI-2 interface standard, according to product marketing manager Sheryl Lewis. These models, each designated by the suffix S, as in ProDrive 120S, also feature Quantum's Advanced SCSI Application Package to speed data retrieval and enhance overall system performance.

The new models meet the requirements of desktop work stations with their average seek times under 15 ms and burst data-transfer rates of up to 4 Mbytes/s. Included are optional aspects of the SCSI-2 standard such as command queuing and cache-control parameters, as well as zero rotational latency reads and writes.

Areal Technology's MD-2020 drive stores 49.2 Mbytes on a 2.5-in. hard disk. It weighs 4.8 oz.

Still kicking up its heels after all these years, the venerable data-cassette memory backup is getting a boost from a new model offering four times the capacity and twice the speed of earlier versions

Both the SCSI and AT-Bus ProDrives feature an enhanced version of Quantum's proprietary DisCache disk-caching technology and a 64-Kbyte on-board buffer. The enhanced DisCache employs an adaptive prefetch strategy so that the prefetch algorithm can be tailored to the access pattern of the operating system, optimizing cache performance. In typical applications, DisCache improves disk access times by 35%, from less than 15 ms to less than 10 ms. The mean time between failures exceeds 50,000 hours.

In quantities of 100, the drives sell for $880 to $1,250, depending on capacity. Quantum, which recently converted its production from 5.25- to 3.5-in. units, says that production models of its 120S and 170S are now shipping, and that evaluation units of the others will be available this quarter.

As might be expected, the 5.25-in. disk-drive world is not sitting still. It makes a big jump in storage capacity with Maxtor Corp.'s new Panther family of drives that store up to 1.67 Mbytes unformatted. The family consists of Panther 1 products, with ESDI, IPI-2, and SMD-E interfaces, and Panther 2 products with embedded SCSI-2 controllers. Command overhead is less than 500 μs and average seek time is 13 ms. Short seek performance of 2 ms track-to-track is the fastest in the industry, says the San Jose company.

In particular, Maxtor is aiming the Panther 1 with its 50,638 bytes/track and 1,778 cylinders at replacing 8- and 14-in. disk drives. The Panther drives offer unformatted storage of 0.8, 1.2, and 1.3 Gbytes.

They feature low command overhead of less than 5 μs and transfer rates of 22 and 24 Mbits/s. Panther 2 products have unformatted capacities of 0.8 and 1.22, as well as 1.67 Gbytes. Calculated MTBF is 100,000 hours.

One of the industry's oldest small-computer backup technologies—data cassettes—is also enjoying a capacity jump. TEAC America of Montebello, Calif., says it has quadrupled the highest available backup capacity of the quarter-inch tape cassettes by putting 600 Mbytes in a 3.5-in., half-height form factor.

With a 60-in./s tape speed and 242-Kbyte/s data-transfer rate, the model MT2ST/N operates at nearly double the rate of earlier cassettte drives. This rate—which is on a par with more expensive 8-mm helical scan drives, according to product marketing manager Michael Helsel—means the drive can back up 600 Mbytes of data in 40 minutes.

The new unit achieves its capacity not by data compression but through more careful design of its electronics and mechanics. Indeed, the drive relies on the same double-density recording method and group-coded recording 4/5 encoding scheme as its 160-Mbyte predecessor.

For one thing, the data-recording format has been modified slightly to preserve read-after-write verification at the higher density. And the company's two-track, dual-gap ferrite read/write head has been enhanced to slice 15% off the write track width, 35% off the read track width, and 30% off the gap length.

The result is to increase the number of recording tracks from 17 to 21, and recording density from 24,000 flux reversals/in. to 48,000. Additionally, TEAC employs a higher-density tape formulation to help boost backup capacity. ☐

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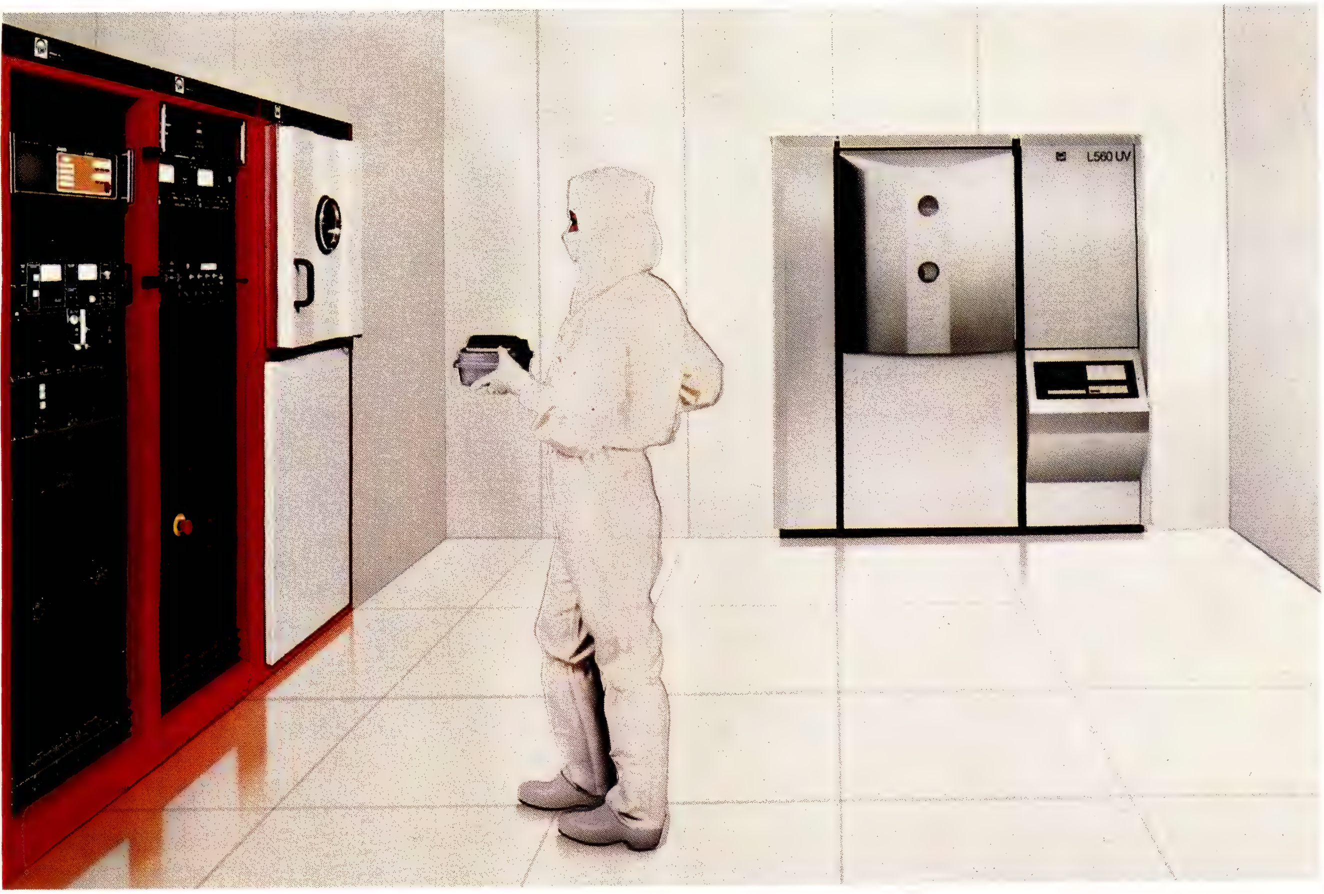

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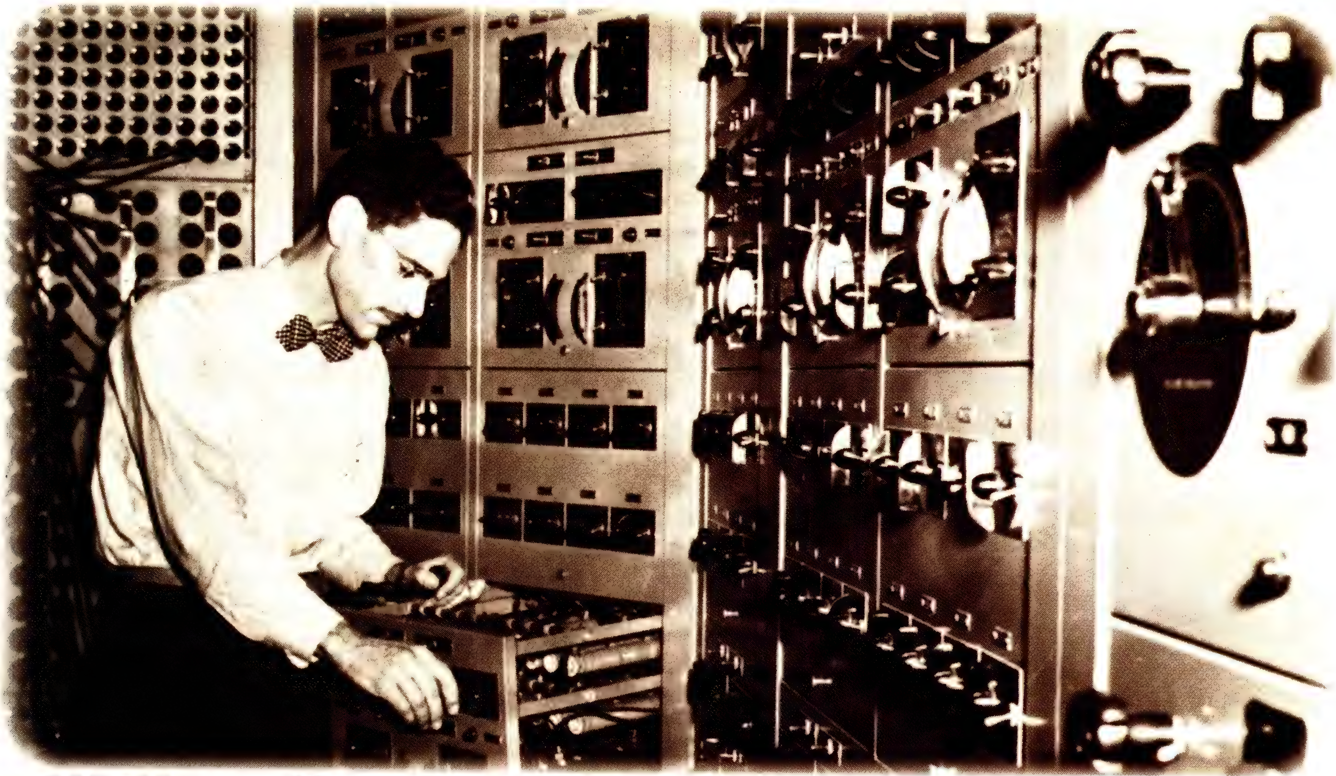

We Were Already A Sizable Force In Technology Back When Technology Itself Wasn't Exactly Small.

It was so early in the evolution of electronic computation that the word "computer," in its modern sense, had yet to enter the language. Still, in 1946, the big news at the Georgia Institute of Technology was very big indeed: the arrival of one of the nation's first AC network calculators.

In the decades that followed, while the gigantic new computing machines were shrinking to the size of credit cards, technology itself was growing rapidly in Georgia. Today engineering R&D expenditures at the public-university level are the highest in the country, and the state is the Southeast's second fastest-growing center of technological employment.

Meanwhile, Georgia's traditional university-industry partnership continues to flourish. In programs designed to provide fledgling high-technology companies with crucial start-up services and incubator facilities. In cooperative projects set up to address the specific needs of the private sector and to expedite the transfer of basic research into the marketplace.

Not surprisingly, along the way, Georgia has developed some of the nation's most sophisticated transportation and communications systems. More surprisingly, however, labor costs have remained moderate, and corporate income taxes haven't been raised since 1969.

So write on your letterhead or send your business card to John Boothby, Georgia Department of Industry, Trade & Tourism, Dept. ELE, P.O. Box 1776, Atlanta, GA 30301. Or call us at 404-656-9306. And find out how Georgia's strong technological base can help you manage some important numbers of your own:

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Circle 152

LOOKING AHEAD TO FDVDI

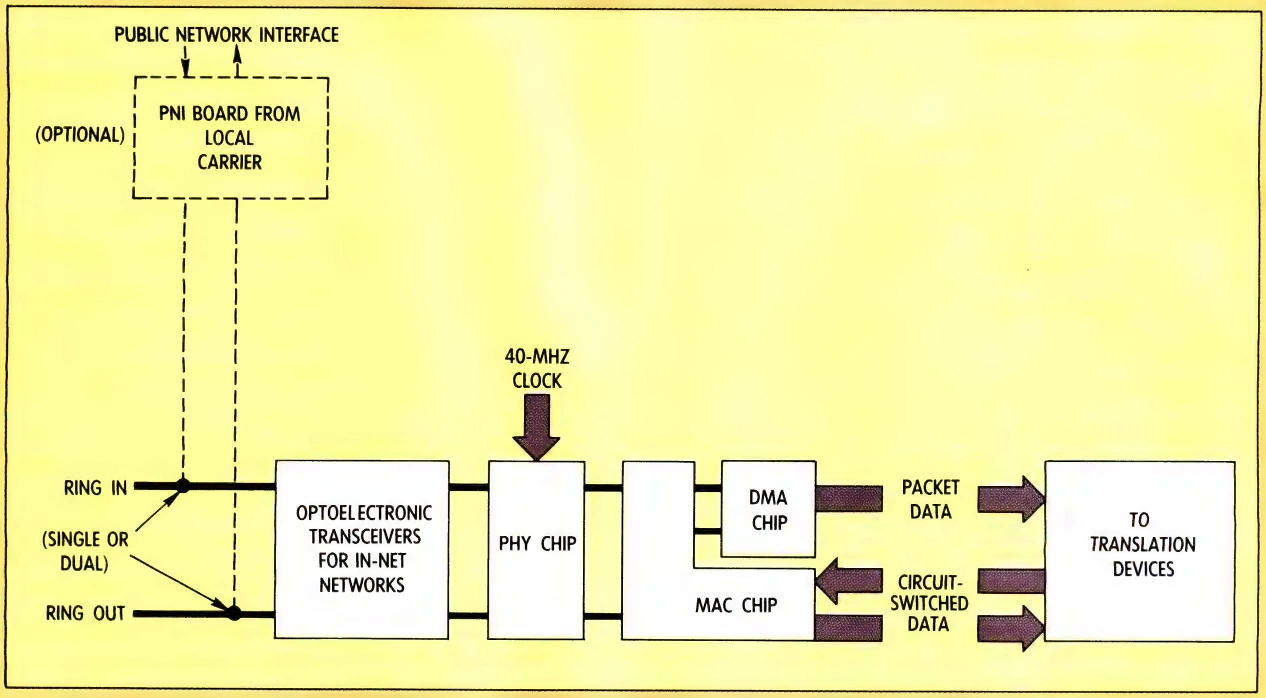
A proposed next-generation standard, FDVDI, can fully integrate voice, data, and video transmission, says a chief backer

BY SAMUEL WEBER

The Fiber Distributed Data Interface standard has barely been set in place, but one purveyor of fiber-optic network products is already campaigning for a next-generation standard—and is ready to unveil a chip set to implement it.

In-Net Corp. of San Diego is aggressively promoting the Fiber Distributed Video/Voice Data Interface, an extension to FDDI that corresponds to the first two layers of the seven-layer Open-Systems Interconnection reference model. According to In-Net, FDVDI accommodates both circuit-switched and data services on the same ring and can provide fully integrated data, video, and voice communications. Such integration is crucial to the full exploitation of newly emerging information technologies, the company says. The

CONCEPTUAL FDVDI STATION



In-Net's three-chip set can implement an integrated private data/voice/video network that ties into public transmission facilities. It addresses the physical-layer interface (PHY), media access control (MAC), and direct memory access (DMA).

proposed standard also enables private networks to link up with public networks operating company facilities in emerging metropolitan-area nets.

In-Net is not alone in its push to make FDVDI a standard. ASCOM-Hasler AG of Switzerland has asked the European Telecommunications Standards Institute to consider adopting FDVDI. Nor is FDVDI the only next-generation fiber-network standard being promulgated. FDDI-II, now under discussion in the American National Standards Institute's X3T9.5 committee, extends FDDI beyond its existing 100-Mbit/s limit.

But FDVDI can interface more readily with the synchronous digital transmission facilities of North American and European telephone companies than can FDDI-II, says John Mazzaferro, In-Net's director of marketing. That's because the FDVDI ring operates at a range of transmission rates: 34, 45, and 140 Mbits/s. This span enables private networks to link with public networks to create metropolitan-area networks.

"Right now, FDDI-II is up in the air," Mazzaferro contends. "Private-branch-exchange vendors want it one way and international groups want it another way. We've taken the most practical implementation route."

FDVDI's circuit-switched service offers multiple channels for synchronous full-duplex transmission of video and voice. These channels, each operating at 64 Kbits/s, can be combined for higher transmission rates, up to the maximum rate supported by the ring.

In-Net is not alone in pushing FDVDI, but others are lobbying for a competing fiber-network standard

The FDVDI data service at the client interface is identical to that provided by the ANSI X3T9.5 FDDI standard. Because of its robust protocol, FDVDI can be a backbone network for local-area networks conforming to the Institute of Electrical and Electronics Engineers' 802.3, 802.4, and 802.5 LAN standards, as well as for FDDI.

On an FDVDI ring, total available transmission bandwidth may be allocated between the circuit-switched and packet services according to the immediate needs of each service. This function, which can be performed dynamically without disrupting established circuit-switched services, helps maximize the use of bandwidth on leased digital transmission services.

"That's one of the key features," offers Guy Crauwels, director of In-Net's research and development test site in Deerfield Beach, Fla. "If you allocate all the bandwidth to the circuit-switched service, the upper limit is close to 140 Mbits/s. Essentially, all the bandwidth is available for circuit-switched service."

In-Net is implementing the FDVDI protocols in a three-chip set that addresses the physical-layer interface, media access control, and direct memory access. All three chips are being built with high-density CMOS, 1.5-μm, sea-of-gates technology; Toshiba Corp. of Tokyo makes the chips for In-Net. "We're willing to sell the chip set or license it for a nominal fee," says Crauwels.

Prototypes are now being tested at In-Net's R&D test center, and the set is slated to be demonstrated at the Cebit industry show in Hanover, West Germany, next March. "We're putting the chip set through its paces," says Crauwels, who adds that the set should be available in the first quarter of next year.

"We're targeting large-bandwidth clients using modern work stations, especially for computer-aided-design applications," Crauwels says. "We're aiming at the larger companies that have large campuses and that need to distribute these kinds of services throughout their organization. We can provide real-time data transmission with guaranteed delivery—not data subject to token availability."

In-Net plans to use the chip set in its own system products. If FDVDI emerges as a standard, the company says, it will offer the technology to others. ☐

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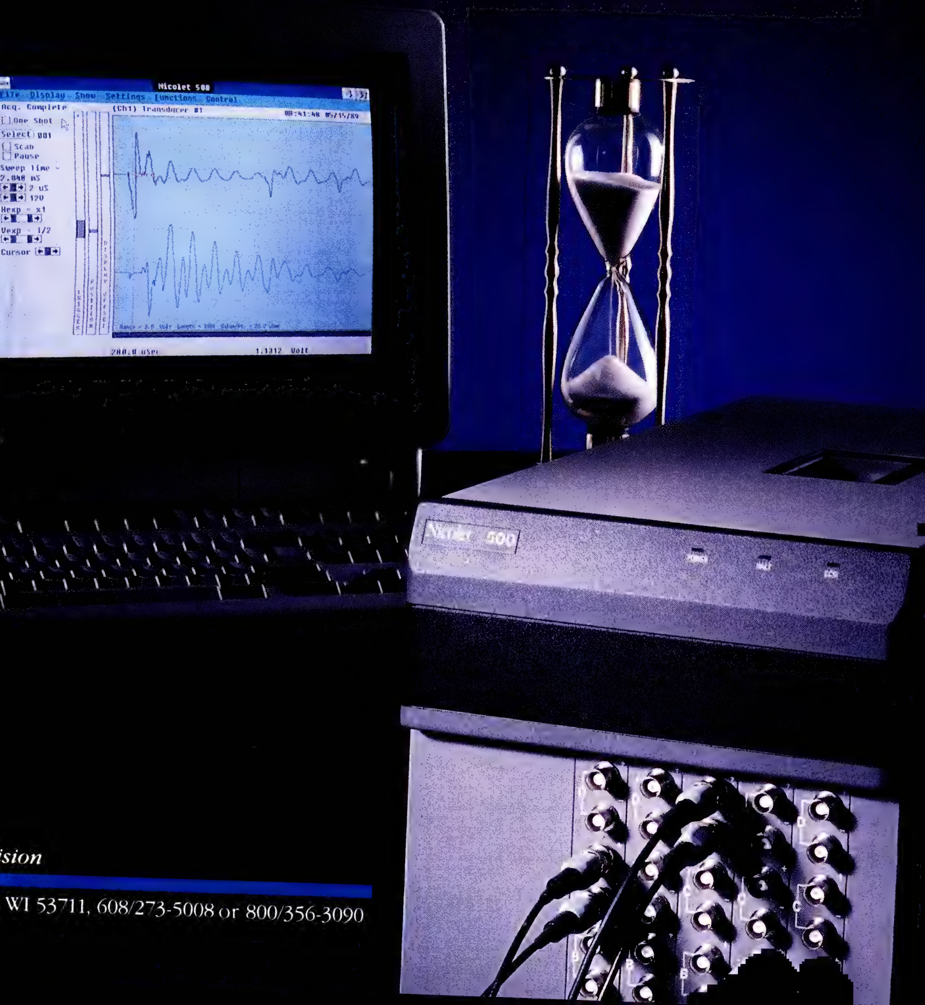

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THIS PRINTER TAKES ON PM GRAPHICS

BY TOM MANUEL

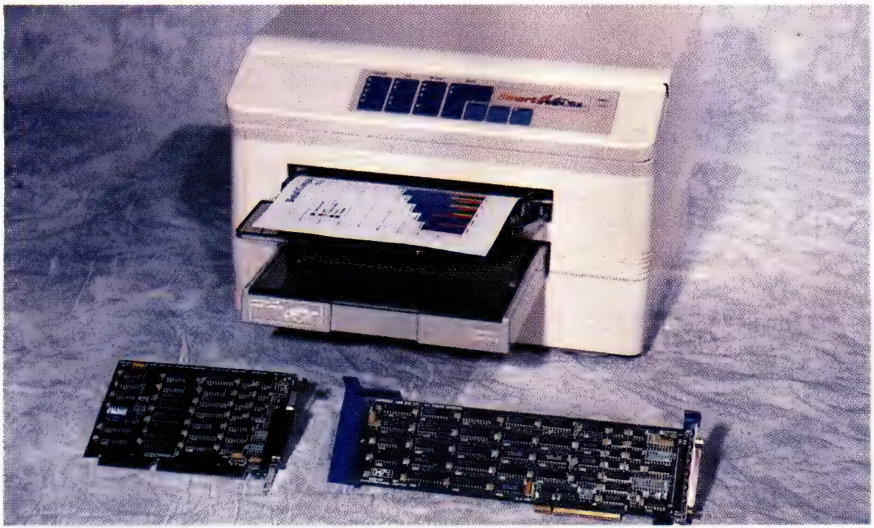
QMS unveils the first system to directly support the Presentation Manager imaging model

Computer operating environments like the Microsoft/IBM Presentation Manager hold out the promise of printing advanced graphics exactly as displayed on the screen. To fulfill that promise, however, printers must directly support the Presentation Manager Graphics Programming Interface imaging model. QMS Inc. would like to cash in on this emerging market by being first with a line of OS/2-Presentation Manager printers.

Key to the Mobile, Ala., company's solution is an embedded controller that supports the what-you-see-is-what-you-get, or wysiwyg, environment from display to printer output. The controller board is built around a Texas Instruments Inc. TMS34010 graphics processor running at 50 MHz and four proprietary application-specific integrated circuits. Early last month, QMS began shipping preproduction units of the controller with a 300-dot-per-in. thermal transfer color printer, along with a software development kit. Versions are available for IBM Corp. PC AT and PS/2 computers, and final products will be released by the end of the year. (Users who want to stick with the DOS environment and still get Presentation Manager-level performance can turn to the Exact-2000 controller card from Flanders Research Inc. of Flanders, N. J. It delivers 1,600-by-1,200-pixel resolution, scalable printer and screen fonts, and compatibility with industry-standard Postscript software [*Electronics*, October 1989, p. 23].)

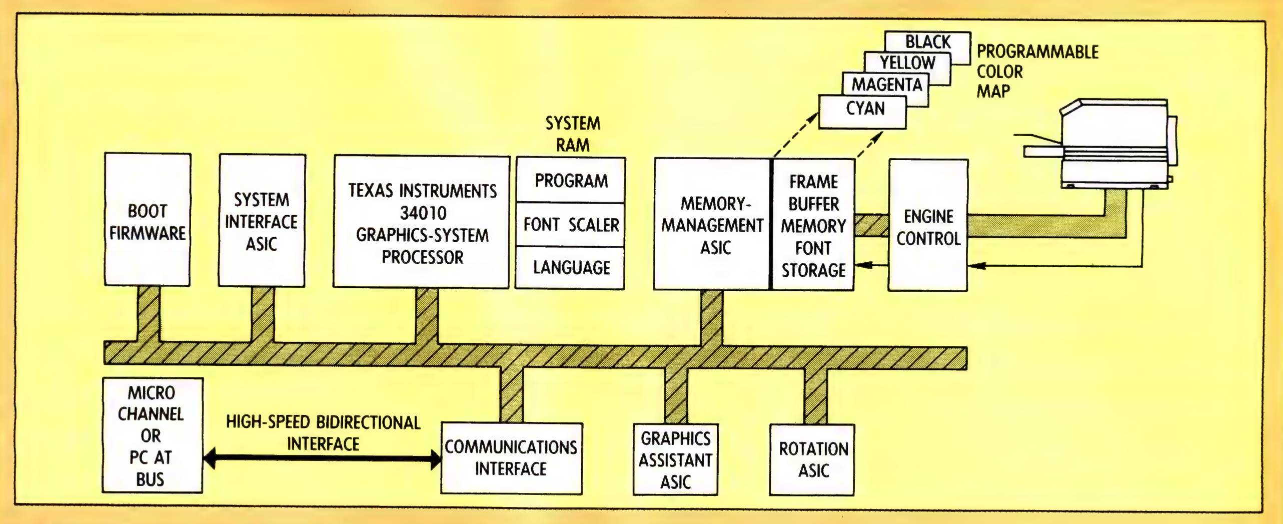
For PM graphics, the computer and the controller must be able to drive the printer at top speed—in QMS's case, a blazing 8 pages per minute. In addition, the printer must accurately render on paper the imaging model displayed on the screen. Unified imaging models provide the kind of correspondence between printer and screen needed for this job, and a number of wysiswyg printing and display systems using such models already exist for other computers. Among them are Adobe Systems Inc.'s Postscript and Display Postscript, along with Apple Computer Inc.'s direct implementation of the Quick Draw display for its printers.

However, if the Presentation Manager imaging model is translated to, say, the Postscript printer, efficiency will probably suffer. "The PM imaging model is very different from the one used by Postscript," and the resulting mismatch plays havoc with efficiency and accuracy, says Donald L. Parker, executive vice president for products and technology



Driving the QMS printer is an embedded controller that supports the "wysiwyg" environment from display to printer output.

CONTROLLER CALCULATES PRESENTATION MANAGER IMAGES



The controller board is built around a TI 34010 graphics processor and four proprietary ASICs. Now set up for Presentation Manager, its programmable design is adaptable to other imaging models as well.

at QMS. The best solution is a system that directly presents the Presentation Manager imaging model to a printer. That is what QMS has done.

"This is new leading-edge technology for printing," says Dano Ybarra, product manager at QMS's Imagen Division in Santa Clara, Calif., which designed and built the controller architecture jointly with QMS in Mobile. Most of the software for the project comes from Graphic Software Systems Inc. of Beaverton, Ore., he adds. Although QMS has chosen to offer the PM/GPI imaging model first, its programmable general-purpose design can be adapted for other imaging models.

GOOD TRADE-OFF. The QMS controller design uses the proprietary ASICs to support and enhance the performance of the 34010. The system gets its clout by implementing the most frequently used GPI calls—the low-level primitives—in the ASICs and leaving the high-level primitives for the 34010 to execute, a job at which it excels. This turned out to be a good trade-off, as seen by the resulting controller's 8-page/min. performance.

The ASICs consist of graphics assist chips, a rotation IC, a memory-management chip, and a system-interface IC.

The graphics assist adds some data-management functions in hardware that the 34010 doesn't have—mainly some color-processing functions such as a full three-operand block-transfer operation. The graphics assist chip acts as a coprocessor to the 34010. The low-level graphics and color primitives are offloaded from the 34010 to the graphics- assist ASIC processor.

The system-interface ASIC manages the dual-memory, dual-bus architecture of the controller. The memory architecture includes the private system memory on the 34010 and the frame-buffer memory on the controller board.

The dual-bus structure includes the main system bus and a high-speed bidirectional interface to either a Micro Channel architecture or a PC AT bus. The dual-memory, dual-bus structure means that the system does a great deal of parallel processing, which boosts performance.

As implied by its name, the memory-management ASIC performs demand-paged memory management of the frame buffer and system memory. The system has 1.2 Mbytes of frame-buffer memory, enough to generate the whole page bit map. The controller generates a page in its entirety before sending it to the printer.

The intelligent memory-management ASIC uses its smarts to manage the frame-buffer memory. After sending a page to the printer, it does not have to wait 8 seconds before it can start building the bit map for the next page. When it builds a page, the ASIC notes which parts are white space and does not use those parts of the bit map. Once it sends a page, it can start building the next page in the parts of the bit map not used for the previous page. The standard configuration of the QMS PM/GPI printer controller will have 2 Mbytes of memory. Up to 6 Mbytes of expansion memory may be added for the queuing up of more pages.

The rotation chip, also called the scanner ASIC, provides the interface between the frame-buffer page memory and the printer engine. This ASIC relieves the front-end software of basic tasks of driving the printing engine and doing the color separations.

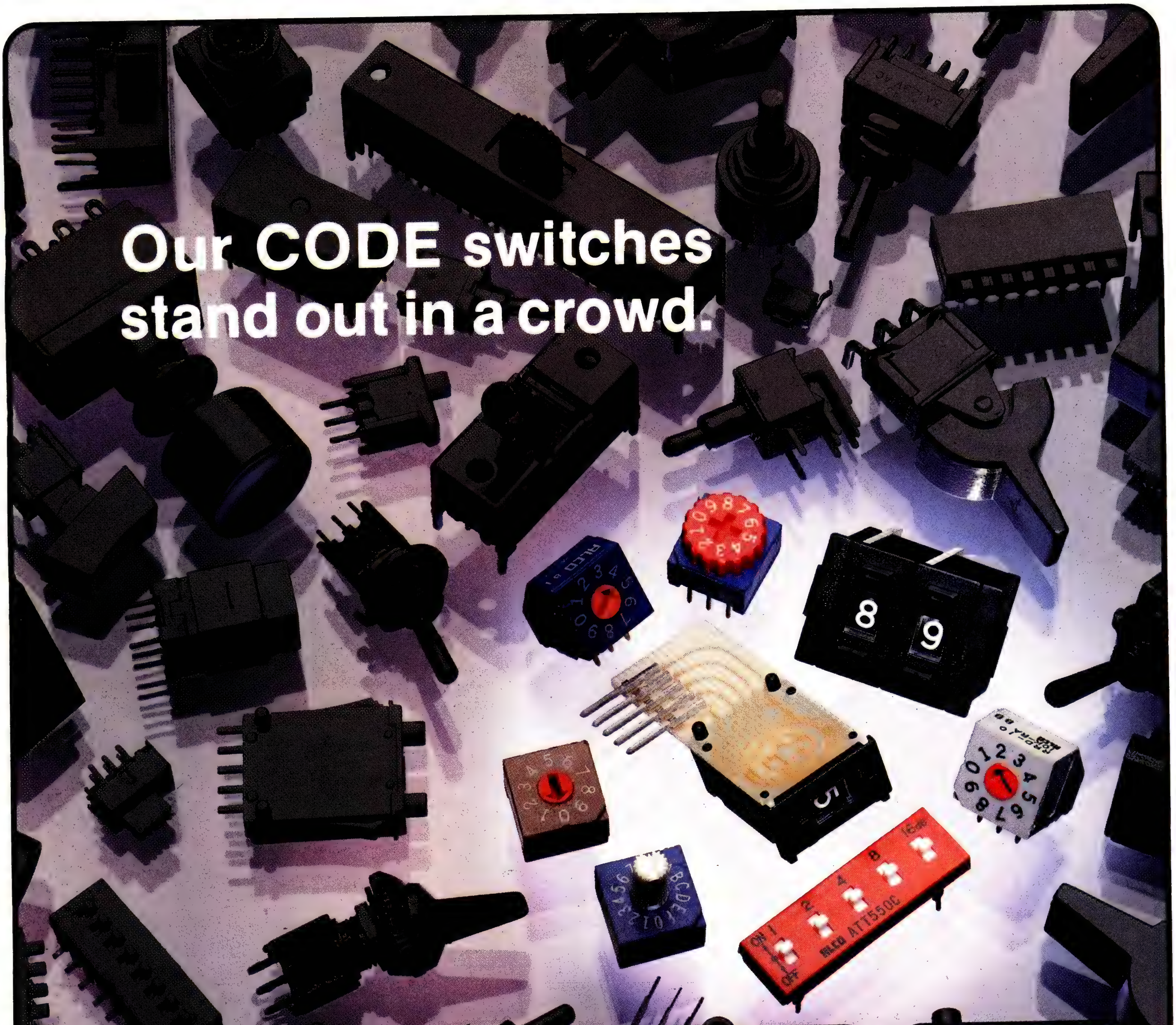
When the 34010 starts up, it can read software into its system memory. The entire printer system firmware is loaded into the 34010 system memory from the host's hard disk upon the initialization of the printer.

FLEXIBILITY. This makes the PM/GPI controller a flexible, programmable engine. It does not have to be run as a fixed design. Software to make it a PM/GPI image-model printer controller can be downloaded from the host system. When QMS chooses to do so, it can provide software that can replace the PM/GPI code and reconfigure the printer for other imaging models. This programmability and the general architecture provide an intelligent controller for any device emulation, language, or imaging model.

Since the QMS PM/GPI controller provides a direct one-to-one match for the GPI environment for the graphics requirements of both the display and the printer, the printer outruns a Postscript printer running off a PM/GPI system with translation. According to Parker, the printer running off the PM/GPI controller runs just as fast as a Postscript printer on a system rendering the Postscript imaging model.

Correctness of the page image as it goes from the screen to the paper is just as important an aspect of performance as speed. Correct rendering, both for color and graphics, is a problem when mapping from GPI to a Postscript printer.

NEC Corp. builds the printer controller's ASICs in CMOS. The graphics-assist ASIC is actually two chips—one with 7,000 gates and the other with 3,000. The rotation ASIC has 7,000 gates, the memory-management chip 5,000, and the system interface ASIC 1,000. ☐



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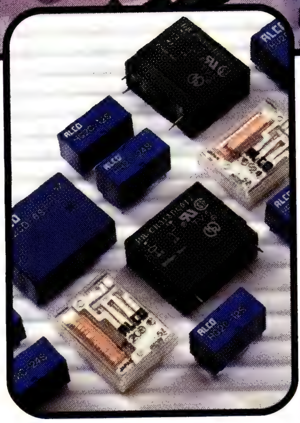
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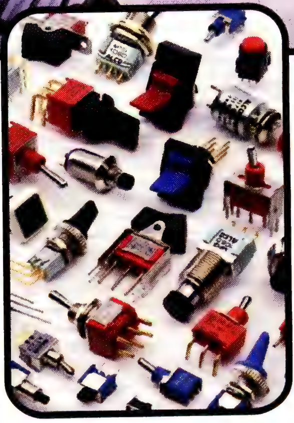
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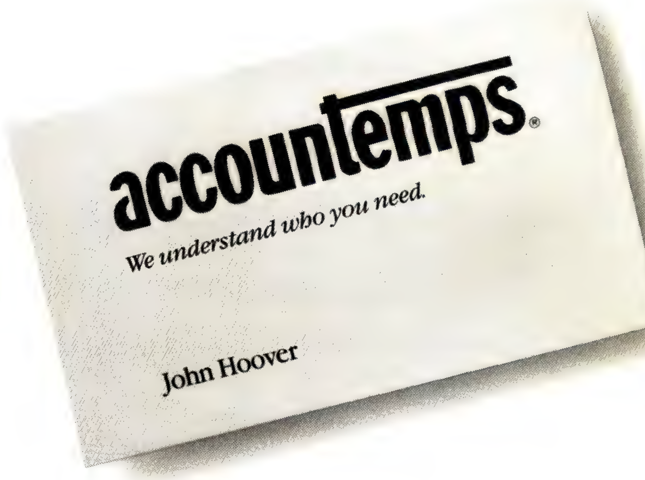

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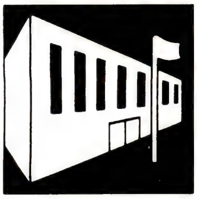
COMPANIES TO WATCH

FLUSH WITH CASH AFTER GOING PUBLIC, CIRRUS HITS THE ACQUISITION TRAIL

Peripheral IC maker hunts board-level products to be replaced by chips



MILPITAS, CALIF.

A company that goes public successfully finds itself with $24 million in cash. What's the next step? For Cirrus Logic Inc., the answer is to go out and buy someone else. "We will identify clusters of competence and acquire them," says Michael Hackworth, president and chief executive officer of the Milpitas-based maker of microcomputer peripheral chips.

The ideal match, he adds, would be "a company making board-level products with software and firmware, where the board could be replaced by a chip or two"—Cirrus Logic's chips, of course.

This zeal to grow by acquisition is not some isolated flight of fancy on the part of Cirrus Logic executives. Rather, it is part of a grand strategy that has seen the five-year-old company's revenues grow sevenfold since 1987, to $36.9 million this year. In that period, the company climbed out of the red, chalking up $4 million in profits in 1989 after losing $6.4 million in 1987 and $8.4 million in 1988.

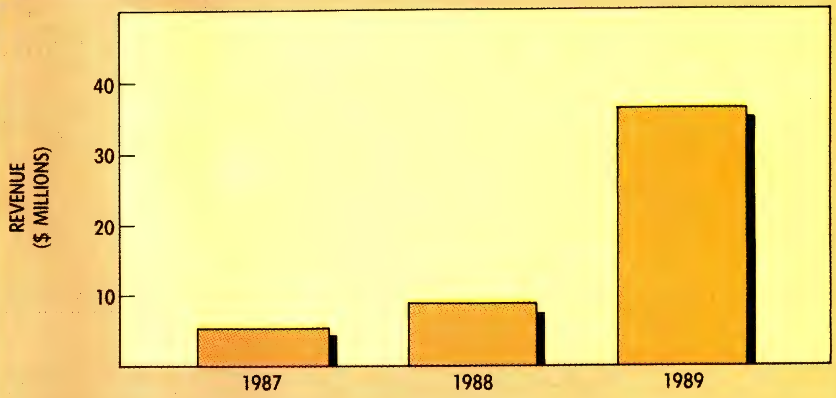
Now Hackworth sees a window of opportunity opening in what he perceives as a widening system-performance gap. "As processor power increases," he says, "the box can't keep pace." The pressure points, says Hackworth, are memory, logic, and peripheral control logic. It is in the last area that he detects an opening.

The market for peripheral control logic chips was $3 billion in 1988, according to Dataquest Inc. of San Jose, Calif. "That's the market we're aiming for," says Hackworth. His four major targets:

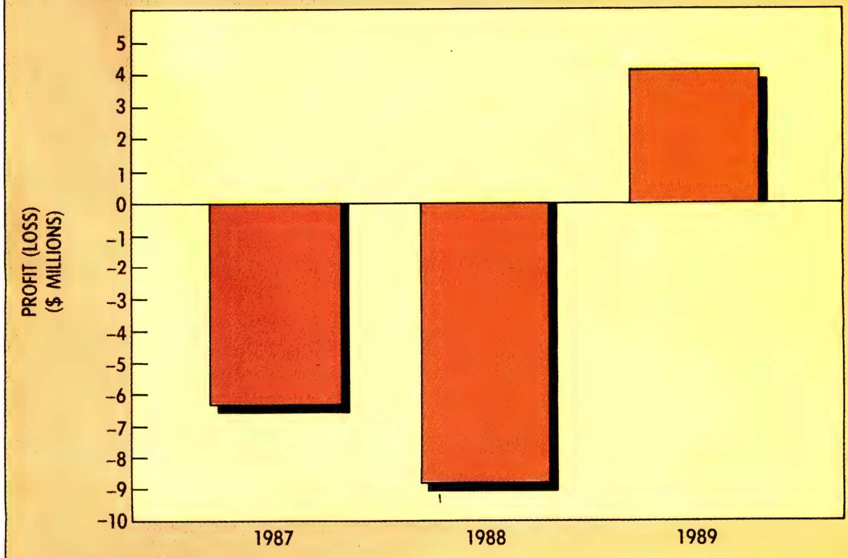
- **Mass storage.** "There is a trend toward intelligent drives," says Hackworth. He puts the market at 20 million units a year by 1991.
- **PC graphics.** This market has been opened by the transition from the EGA standard to VGA, which was introduced by IBM Corp. in its PS/2 machines. Cirrus Logic technology emphasizes complete backward compatibility with graphics standards. Also important: the emergence of the laptop computer, with its need for storage that can operate off a battery, and the appearance of quality displays for such machines. In the past year, says Hackworth, Japanese companies have shipped liquid-crystal displays with good resolution; Cirrus Logic's edge is a chip that converts color to monochrome for this new breed of screen.
- **Data communications.** Here the target is the central computer with many terminals in a network.
- **Printer graphics.** This market is growing tremendously as desktop publishing continues to invade the business world.

All this activity is fueled by last June's initial public offering of stock—some 3.34 million shares—that sold out quickly. "The timing was good," says Hackworth. "Technology shares had been beaten down, and the market was hungry for some." Now he wants to find some companies that need nourishment from Cirrus Logic's war chest. *–Howard Wolff*

CIRRUS' REVENUE SOARS . . .



. . . AS PROFITS START TO CLIMB



SYNOPSYS: THE RIGHT TOOLS AT THE RIGHT TIME

MOUNTAIN VIEW, CALIF.

With an impressive winning streak, Synopsys Inc. is one of the hottest startups in Silicon Valley. Making its record even more impressive is the fact that the Mountain View company's success has come in a state-of-the-art technology—design synthesis—that has frustrated other outfits. But that very success has produced an irony: Synopsys is now a prime takeover target in an industry that is seeing a rash of such activity.

Synopsys has managed to be in the right place at the right time with the right technology. Its design tool provides recognizable benefits and can be used by designers as soon as they buy it, with no need for retraining.

The results are reflected in the company's healthy bottom line. "Synopsys is growing at a rapid pace," says Robert Herwick, senior technology analyst at Hambrecht & Quist in New York. "It has a current revenue rate of over $10 million a year and is booking new business at a rate of $15 million a year. The company has been profitable for the past three quarters and has been generating cash for the past two quarters."

The man behind the technology is Aart de Geus, company founder and senior vice president of engineering. De Geus says that to sell a new concept such as synthesis, a product must be easy to use and provide an immediate return on investment. Synopsys' first product, called the Design Compiler and brought out in 1987, allows a designer to input existing netlists—for example, a design currently implemented in discrete components—from which the tool automatically produces an optimized circuit that can be implemented in an application-specific integrated circuit.

But the tool makes a more important mark in meeting the second requirement: it automatically improves the design, making it smaller and faster, in a fraction of the time in which a designer could do the job by hand.

Design Compiler is finding a big audience, according to Synopsys. The company has more than 50 customers and 90 installed seats in three major market segments—computers, communications, and semiconductors—says Robert Dahlberg, marketing manager.

The company's second product, HDL Compiler, is slated to begin shipping next month. It synthesizes an optimized circuit from a design described in either Verilog, a high-level description language from Gateway Design Automation Corp. of Westford, Mass., or the VHSIC High Level Description Language (VHDL), which the U. S. Department of Defense recently specified for all government contracts.

Running the store at Synopsys are president and CEO Harvey C. Jones, left, and founder and technology guru Aart de Geus. De Geus helped develop the company's first product.

De Geus says that 70% of the company's installed base has already ordered the Verilog version of the HDL Compiler. "These users are not simply trying out HDL synthesis," de Geus asserts, "they are building real circuits. A couple are building designs with over a million gates using HDL synthesis."

The Synopsys tools evolved out of Socrates, a logic-synthesis tool developed by de Geus and a group of researchers at General Electric Co. in Research Triangle Park, N. C., in the early 1980s. In 1986, when GE was in the midst of shedding its high-technology assets, it gave de Geus and six members of the Socrates team seed funding for what was then called Optimal Solutions Inc.

GOING WEST. In November 1987, the company moved from Research Triangle Park to Mountain View—"the center of the technology universe," says de Geus—and changed its name to Synopsys, short for "synthesis and optimization systems." De Geus believes the move to Silicon Valley gave the company access to management talent it would not have attracted in North Carolina.

For instance, de Geus recruited Harvey Jones, a cofounder of Mountain View-based Daisy Systems Inc., as chief executive officer. Jones brought to the company his extensive knowledge of the ASIC business and his contacts in that segment, says Peter Schleider, a partner with the investment firm of Wessels, Arnold & Henderson in Minneapolis. Jones masterminded a string of relationships with ASIC vendors, giving Synopsys a strategic advantage over other logic-synthesis companies.

The ASIC deals are vital to Synopsys' success. With logic synthesis, the designer creates a design in a high-level language and the tool creates an optimized gate-level description. For the design to be implemented in silicon, the gates that the synthesis tool creates must map into gates in an ASIC foundry library. The designer or synthesis companies can create the libraries for individual foundries, or the foundries can create them for the synthesis companies.

Having the ASIC supplier create the library ensures the most up-to-date design information and thus the best silicon implementation. Nine ASIC suppliers have agreed to support the Synopsys tool: Fujitsu, Harris, LSI Logic, Motorola, National Semiconductor, NEC, Seiko, Signetics, and Toshiba (see p. 56).

The task that Synopsys' management team now faces is to put the company in a position to grow beyond its one-product status. Jones believes Synopsys can grow and remain financially healthy, but analysts wonder if the company can maintain its independence. Some see a parallel between Synopsys and Verilog developer Gateway Design Automation. In the process of issuing its initial public offering, Gateway chose instead to be taken over by Cadence Design Systems Inc. of San Jose, Calif.

Many Wall Street investors already have decided the outcome of the Synopsys scenario. "If Cadence doesn't own Synopsys in two years, there is something wrong," says Herwick of Hambrecht & Quist. That sentiment is echoed by others following the computer-aided-engineering business. One reason: Synopsys and Cadence already have estab-

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But the more fundamental reason that a takeover is likely, says analyst Schleider, is that Synopsys will have to become a broad-based CAE tool supplier to compete with two powerful competitors coming on the market. Mentor Graphics Corp. will soon introduce a synthesis product that it acquired last year when it bought Trimeter Technologies Corp. Silicon Compiler Systems Corp. is another competitor with a formidable logic-synthesis offering.

In de Geus's view, however, the greatest competition is not other ASIC logic-synthesis companies but in-house tool-development groups that have purchased licenses for the technology from the University of California at Berkeley. These groups are now developing their own synthesizers.

Synopsys executives say they have no intention of selling out or any need to do so. They point out that Synopsys is profitable and has new product plans that will continue its profitability into the foreseeable future. *–Jonah McLeod.*

IT'S ONE-STOP SHOPPING AT WESTERN DIGITAL

IRVINE, CALIF.

In an impressive turnaround for a company that nearly dropped off the industry scope for several years, Western Digital Corp. is quietly reaching some attention-getting goals. Perhaps most eye-catching: sales will reach almost a billion dollars in fiscal 1989.

In the process, Western Digital has successfully put into place the apparatus needed to carry out a grand strategy defined more than five years ago by chief executive officer Roger W. Johnson. The Irvine company's ambitious plan is to become the one-stop shopping source for personal-computer manufacturers. That means supplying much of the key hardware they need—chips, boards, and subsystems—except for microprocessors. It also means that Western Digital, by choice, is out of the spotlight that falls on the glamorous business of building the entire PC or a high-visibility processor.

As a result, few observers outside the PC business itself bothered to notice what was afoot at Western Digital as the company set about to become nothing less than "the Delco of personal computers," in Johnson's words. His allusion is to the General Motors Corp. subsidiary that is a premier supplier of electrical and electronic parts for autos and trucks.

PLAN WORKED. How well the strategy has worked can be judged from Western Digital's growth since Johnson took over in 1983, when sales totaled $30 million, mostly from data communications chips. The company now has a dominant role in some key PC niches. The bedrock line is storage-management controllers and chips, whose sales amounted to nearly $450 million in fiscal 1989. The latest to be added to the mix are disk drives, procured in the 1988 acquisition of Tandon Corp.

Even faster growth comes from video imaging based on graphics chip sets, where sales zoomed to about $250 million this year from $21 million in 1986. In this market, Western Digital has locked up more than 60% of original-equipment-manufacturer sales. Also coming along fast is the company's original niche in communications. Western Digital last year advanced into the No. 2 position as Ethernet supplier behind 3Com Corp. It ranked sixth a year earlier.

With all these pluses going for it, why has the company chosen to keep such a low profile, doing little promotion or advertising? One reason is the dizzying rate of structural and product evolution. "It takes time to digest all this growth," says one Western Digital executive.

But more important is skepticism on the part of the investment community about whether Western Digital can manage its growth. That is laid by company insiders to the uncertainties that go with rapid change. And those, in turn, put the company in a position that is not uncommon among high-technology outfits: it has not been able to meet analysts' rosy profit forecasts—forecasts made with at least the tacit guidance of company executives.

The company's grand strategy is to become 'the Delco of personal computers'

Johnson, who also holds the titles of chairman and president, concedes that the tab for reshaping the company proved much stiffer than expected, resulting in lower profits. The bottom line was hit in particular last year by some $80 million in capital expenditures to upgrade design and production. That came on top of the acquisition of five companies, moving Western Digital into many new factories in 26 countries. "I didn't properly assess the cost in the short term," Johnson admits. Still, Western Digital stayed in the black, and has enjoyed 20 consecutive profitable quarters.

Moreover, the company still boasts some backing on Wall Street despite the run of recent disappointments. Says Needham & Co. analyst Raj Rajaratnam, "The strategy is a good one, and Roger is a good strategic thinker. But the execution is not stellar, shall we say."

BUMPY RIDE. John F. Geraghty of New York's First Boston Co. is one financial seer who thinks better profits lie ahead: "We'll probably begin to see vindication as far as earnings growth is concerned." But he calls the stock price's nosedive from above 13 to below 8 in 1989—during a period when he was recommending it—"not exactly a cheery ride."

Johnson and his crew of top executives also think the stage is set for Western Digital finally to start showing its true colors. Now the trick is to bear down and "manage the business well," says Kathryn A. Braun, one of those who will have to do just that. She is senior vice president and general manager of Western Digital's biggest business, the Storage Management Group. The performance of Braun's operation is pivotal. "That's where the leverage is—the largest swing factor in earnings is the drive business," says Rajaratnam.

Also, the company has been losing money—an estimated $15 million last year—selling the old-style slow drives inherited in the Tandon acquisition. But all effort has gone into bringing out the new generation of 3.5-in. drives, the Centaur and Caviar lines, that in many ways are the most advanced available. They feature proprietary control circuitry integrated into the peripheral itself and are now being built in quantity.

Braun says she's selling all the new drives the company can make, about 60,000 in the quarter ending in September, ramping up to 100,000 in the current quarter. Moreover, profitability should rise, she predicts, as the full benefits of Western Digital's vertically integrated drive manufacturing start to roll. The company is the only drive manufacturer that can do virtually everything in-house: producing all the chips (which account for 40% of cost), plated media, headstacks, and board assembly.

The trend toward upward integration into subsystems permeates all of Western Digital's plans. Besides disk drives, integration is critical to keeping its market spot as controllers give way to hardware that bundles the advanced interfaces and new functions. Analysts warn that the separate controller business is on the way out, so the company has hustled to have the subsystems ready.

Johnson predicts that effects of the changes will start showing soon and really spur profits upward next year. In retrospect, he is not defensive about the turmoil during the building period. "One man's transition is another man's plan unfolding," he says. *–Larry Waller*

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PEOPLE TO WATCH

STECKEL SEARCHES FOR STRATEGIC PARTNERS

France Telecom gears up for Europe's unified market

NEW YORK

For Marie Monique-Steckel, the great bundling of the European market in 1992 is a two-way street. As president of France Telecom Inc.—she was named to that post in 1979, 10 years after establishing the French government's commercial office in New York—Steckel's job is to sell the state-owned company's ever-widening portfolio of transglobal telecom services to U. S. customers. She is treating the beginnings of a unified European market as a once-in-a-century marketing opportunity.

The premise is simple: if U. S. companies are to do more business in Europe, they will need to communicate with Europe more. France Telecom's 1990 mission statement, Steckel says, commits "70% of our energy and budget to promoting and selling leased-line and integrated network services to multinational U. S. companies."

The remaining 30% of the corporate energy will demand a much higher proportion of Steckel's personal vim and vigor, because it affects the company's strategic, long-term interests. Following the lead of the parent company's European joint agreements, Steckel is busy looking for corporate partners in the U. S.

Minitel—the successful French version of videotex—is her pride and joy. "We have a joint venture with US West on Minitel," she says, "and projects under way with Nynex. We're always looking for alliances with key players here in the U. S." Major opportunities are available in the U. S., she says, because of the divestiture of AT&T Co. five years ago. "We are moving into an era when conventional relationships between companies are breaking down. This is a time when the same company can be your client, competitor, and collaborator."

The unbundling of AT&T occurred just seven years before the bundling of the European market, but the results are expected to be the same—more and tougher competition. "No one realized that the deregulation order in the U. S. would push the [regional Bell holding companies] into Europe," Steckel says. "But competition in the U. S. is quite fierce. I think it makes perfect sense for the [regional Bells] to position themselves outside."

Selling global services to U. S. companies is 70% of Marie Monique-Steckel's mission.

Meanwhile, back in Europe, political forces intent on unbundling the ministries of post and telegraph—commonly known as the PTTs—are stirring. British Telecom, for one, has undergone a drastic degree of deregulation over the past few years. France Telecom is not eager to follow suit. "France is a very state-oriented country," says Steckel. Unlike the U. S., France has had a strong industrial strategy for the past 30 years. Although that brand of national economic behavior is more typically associated with Japanese and other Far Eastern economic powerhouses, "it is something France is very comfortable with," she says.

But perhaps the strongest argument against spinning France Telecom out of the government is financial: "For the past four years, we have given back money to the government to the tune of $500 million per year," Steckel says.

France Telecom has aggressively pursued a program of installing digital lines throughout the country, putting France in a strong position to implement the integrated services digital network. Steckel's job will be to introduce U. S. customers to ISDN services in Europe through France Telecom's leased lines. "We will be ready to implement that by the end of 1990," she says. *–Jack Shandle*

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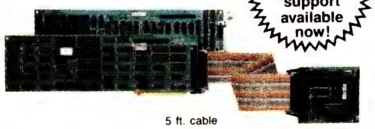

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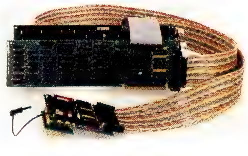

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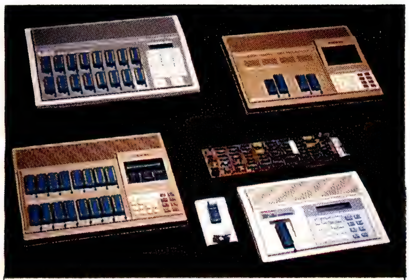

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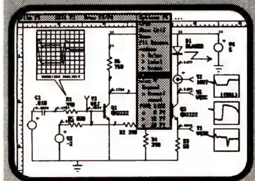

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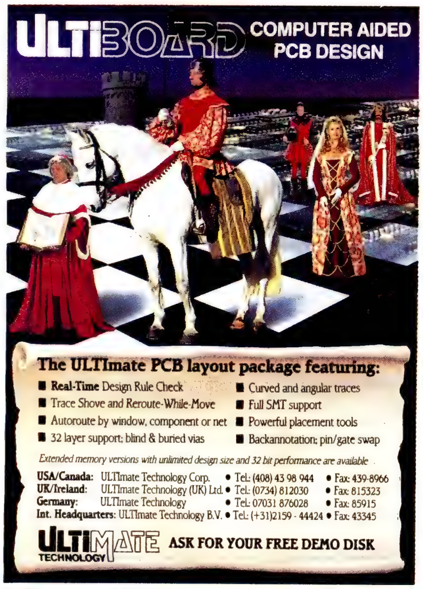

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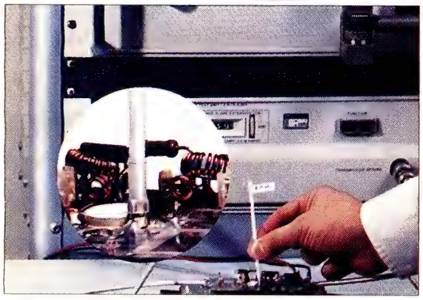

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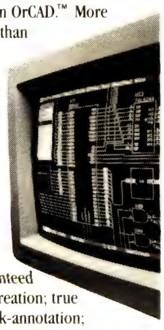

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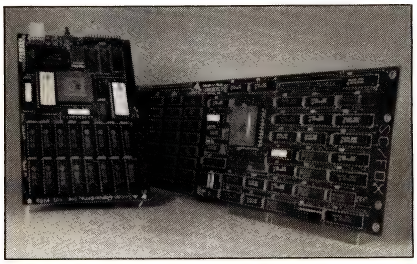

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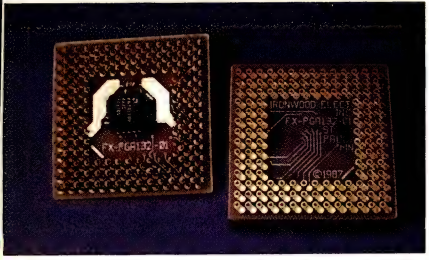

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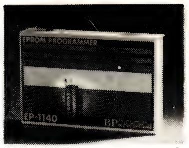

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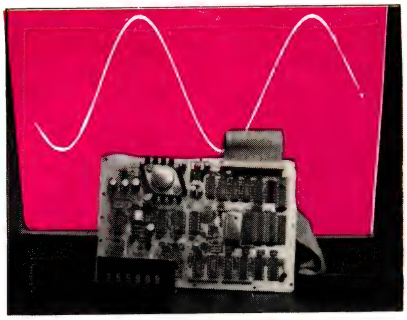

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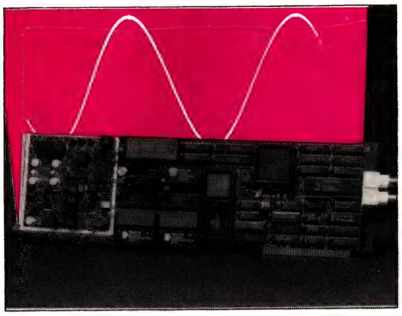

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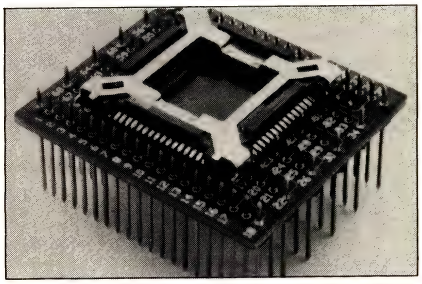

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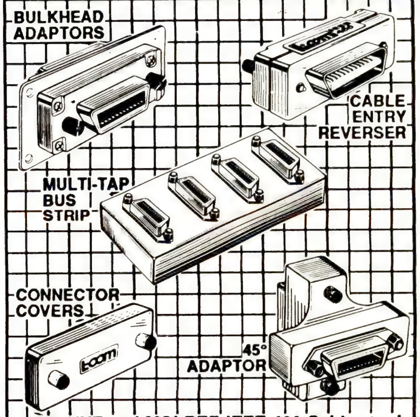

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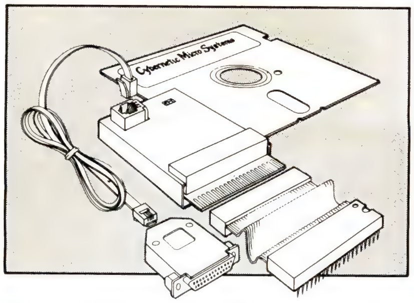

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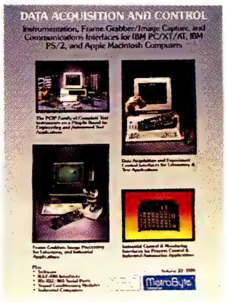

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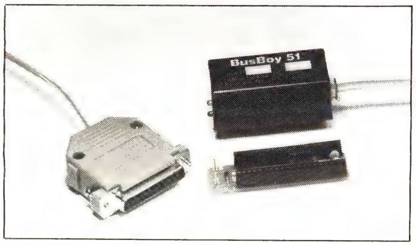

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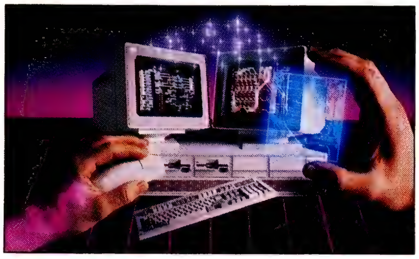

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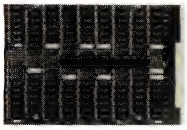

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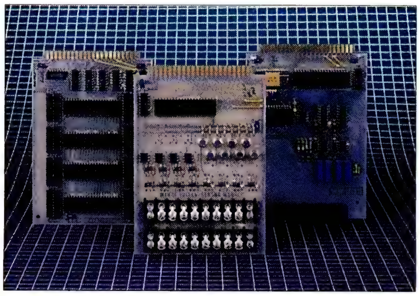

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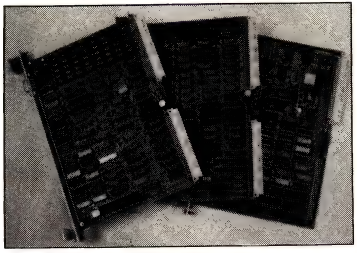

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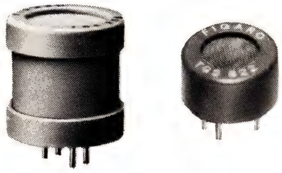

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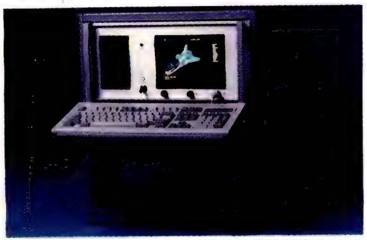

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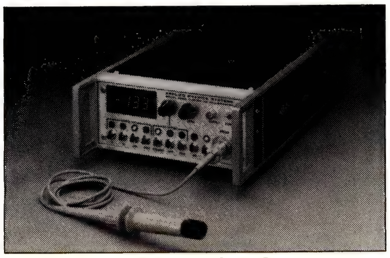

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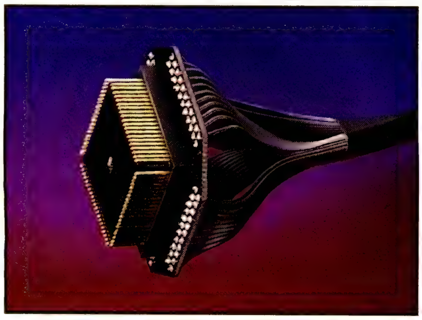

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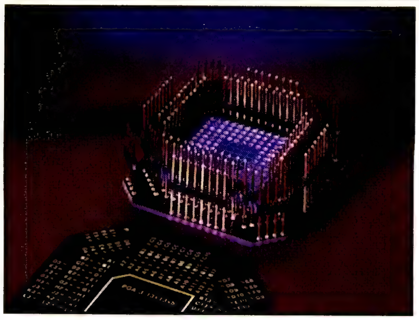

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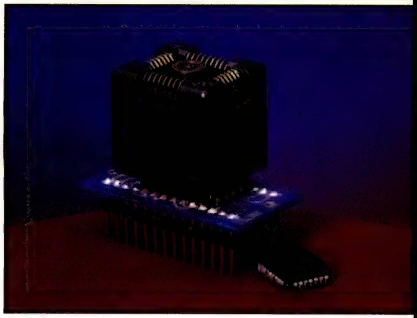

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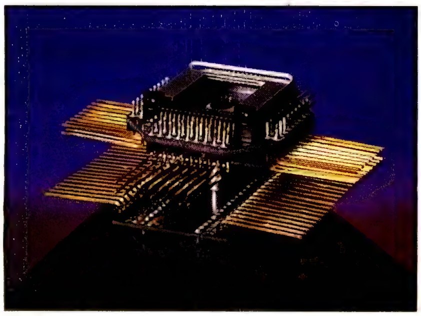

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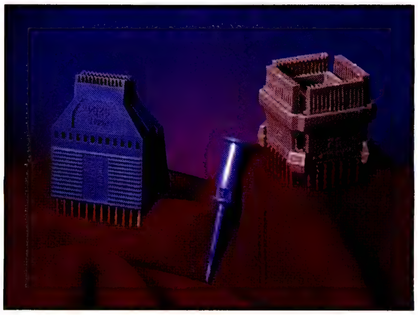

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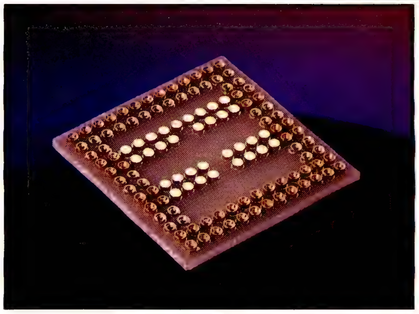

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Abbott Transistor Laboratories	18
ACCEL Technologies	114
Accountemps	106
Actel Corp.	Cov 2, 1
Acculex	117
AMP Inc.	26-27
Advanced MicroDevices	6-7
Advanced Microcomputer Systems	116
American Technical Ceramics	114
Analog & Digital Peripherals, Inc.	117
Antona Corp.	115
Anritsu Corp.	64-65
Applied Physics Systems	117
Augat/AlcoSwitch	105
***Barbados Industrial Development Corp.**	13
BP Microsystems	115
BV Engineering	113
CETRA	66
Clearpoint	Cov 3
Cybernetic Micro Systems	116
Cypress Semiconductor	Cov 4
Daicel Chemical Industries, Ltd.	30
Data Translation	37
Dialight Corp.	9
Emulation Technology	118
Enertec	117
****Epson Semiconductor**	52E
Figaro USA	117
Fuji Polymer Industries Co., Ltd.	80
****FuJitsu Ltd.**	14-15
***FuJitsu Microelectronics**	10-11
****FuJitsu Microelectronik**	10-11
Genrad Inc.	16-17
Georgia Department Industry & Trade	98
Hewlett-Packard Components	60-61
IBI Systems	117
IBM Corp.	74-75
Information Handling Services	91
Infotek	116
Inronwood Electronics	115
Itac Systems Inc.	8
Integrated Device Technology, Inc.	83
Integrad Technologies	117
Intermetrics	73
Intusoft	113
****Krupp Widia GmbH**	69
L-Com Inc.	115
Lambda Electronics	45-52
Leybold AG	97
****Lixi**	13
Logical Devices	115
Logical Systems	116
Matrox Electronics Sys. Ltd.	102
MetraByte	116
Microprocessors Unlimited Inc.	114
Microsystem Service Ltd.	117
Miller-Stephenson Chemical	41
***Mill Max Manufacturing**	25
****Murata Mfg. Co. Ltd.**	52H
Nicolet Instruments Corp.	101
Nohau Corp.	40, 113
Noise Laboratory Co., Ltd.	22
Northwest Airlines	92
Orbit Semiconductor	28
OKI Electric Industries	54-55
P-Cad	21
Performance Semiconductor	84
****Philips Components**	52A
****Philips I&E**	52G, 39
Pico Electronics	31, 43
Promac Div.	113
Pulizzi Engineering	113
****Rohde & Schwarz**	25
RMF Products	116
****Saft**	52C
Sciteq	115
Silicon Composers	114
Specialized Products	114
Spectrum Signal Processing	12
Swissair	42
Techmar Corp.	44
***Teledyne Solid State**	39
***Teradyne**	14-15
Texas Instruments	33-36
Toshiba America Electronic Components	68-69
Ultimate Technology	114
Varta Batterie	109
Vicor	2
Wabash Magnetics	114
Wandel & Goltermann	87
Wiemer's Inc.	114
Wintek	116
***Zehntel Systems**	14-15

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UPDATE: VENDORS CHARGE AHEAD WITH SPEEDIER RISC

Raise your hands, those who did not believe back in 1988 that Intergraph Corp. would introduce a 60-mips Clipper in 1989, as analysts were then saying [*Electronics*, November 1988, p. 104]. It turns out you were right. Keep your hands raised if you also believed that looking forward to such speedy reduced-instruction-set computer chips was asking too much, too soon. Turns out you were wrong.

Bipolar Integrated Technology Inc., of Beaverton, Ore., a specialist in emitter-coupled logic, has been shipping since June limited quantities of a Sparc chip set that can hit 65 million instructions per second at 80 MHz. It does 14 million double-precision Linpack floating-point operations per second.

WORK STATIONS

TECHNOLOGY TO WATCH

WOULD YOU BELIEVE A 60-MIPS CLIPPER? ECL RISC CHIP IS EXPECTED NEXT YEAR

TECHNOLOGY TO WATCH

A 10-MIPS WORK STATION IS HERE FOR UNDER $60,000

Intergraph's RISC-based system outperforms competitive work stations in its price range and offers engineers an extra-large CRT display

Today's competitive work-station marketing environment has systems houses playing a game of mips-manship. The trickiest part is that the game is based on next-generation reduced-instruction-set-computer chips not yet in production.

But one house, Intergraph Corp., plans to ship production versions of its next-generation RISC-based system next month. These work stations, called the 3000 Series, incorporate the Intergraph's new C300 Clipper chips, and are the first to achieve true, conservatively rated, 10-million-instruction/s performance in the class of work stations that cost less than $60,000, according to the Huntsville, Ala., company. The 3000 will easily outperform other current-generation RISC-based work stations in that price range, says Bruce Imsand, vice president of systems development at Intergraph.

In fact, the 40-MHz C300 Clipper chip allows the work stations to pump out up to 13 mips peak, a big increase over the 300 Series work stations, which run at 5 to 7.5 mips. And a 50-MHz version of the Clipper will boost performance to 15 mips next year during the summer.

Part of the performance boost comes from changes in the way load, store, and branch instructions are implemented, as well as changes in the floating-point processor—changes that do not affect software that was written for the earlier version of the Clipper.

December, will cost under $80,000, well below the $90,000 price of the 10-mips, Sparc-based Sun 4. The price difference results from the higher level of integration the C300 Clipper affords. "The C300 consists of four chips: an integer and floating-point processor on one chip, two cache and memory-management chips—one for instructions and one for data—and a clock chip. They all fit on a single card measuring 2.5 by 8 in.," says Eugene Grindstaff, senior manager of work-station sales and support at Intergraph.

"To achieve the equivalent of this [functionality] on other RISC-based systems requires a board of 18 by 15 in.," Grindstaff continues. "Besides using discrete-integer and floating-point processors, these designs use larger emitter-coupled-logic cache memories than the Clipper. They achieve a higher mips rating, but at a higher price, and without necessarily running benchmarks faster than our Clipper-based system."

Intergraph's new system enters into a competitive market. One market research firm, Daratech Inc., based in Cambridge,

Mass., predicts the market will grow 15%. In 1987, it was worth $4.56 billion and this year is expected to reach $5.2 billion. Daratech, specializing in computer-aided design, engineering, and manufacturing, breaks down that total market into three main segments: mechanical, electronic, and AEC (for architectural, electrical, and civil engineering). The lion's share of the 1987 market was held by the mechanical-design segment, at 59%, the electronics-design portion held 22%, AEC made up 17%, and others made up the rest.

Intergraph sells its work stations and the individual boards in them by themselves (see p. 109). It also sells software targeting the three design-automation market areas Daratech describes—mechanical, electronic, and AEC. Intergraph touts the standards they support—Unix System V, Ethernet networking, transmission-control protocol/internet protocol (TCP/IP), and the Network File System, just like the competitors based on Sparc and MIPS Computer chips.

SAME LOOK. Designing the 3000 Series work station was made much easier by the fact that the performance of the new C300 Clipper RISC-chip set looks the same as the C100, from the system's point of view, in all aspects but its clock frequency. But it is not the same. The new work station has a different memory system design, one that can accommodate the 40- and 50-MHz clock rates of the new and future versions of the Clipper chip.

"In addition, the new C300 can perform some functions in the burst mode to make better use of the memory bus than other

A HIGH-THROUGHPUT THREE-PROCESSOR

One chip runs at 65 mips, and a number of companies are shooting even higher

Along with this chip set, the past year has seen plans unveiled for other ultrahigh-speed RISC devices. For example, Intergraph of Huntsville, Ala., says its ECL-based E100 Clipper (referred to as the E1 in last year's *Electronics* article) will be included in a network server due the second half of 1990. And startup Prisma Inc. of Colorado Springs is developing a computer system product relying on a RISC chip built with gallium arsenide. A Sparc licensee, Prisma says little more than that it is "looking at making judicious use of GaAs where it makes sense to do so." However, one industry source speaks of a performance goal that's way out at 250 mips.

In addition, the year has seen good gains in upping the speed and processing power of CMOS RISC chips. CMOS designs operating at up to 100 mips are being contemplated. Also, "old line" microprocessor manufacturers Intel Corp. and Motorola Inc. have both introduced RISC designs.

Such higher-performing RISC chips are the result of developments that usually follow a chip design. Designers have scaled or tweaked their designs as they gained more experience with their processes. Critical paths have been shortened, while compilers and cache architectures improved.

Bipolar Integrated Technology's chip set, made with 10K ECL, consists of an integer unit, a floating-point controller, a floating-point arithmetic logic unit (ALU), a floating-point multiplier, and a register file. The set must operate in an air-cooled environment.

Newest of the chips—and most expensive at $850—is the B5000 integer unit. The price of the three floating-point devices totals $1,710 and the register files, with two needed, come to $740. All together, this adds up to $3,300 per set (in quantities of 100). Sun Microsystems Inc. of Mountain View, Calif., which developed the Scalable Processor Architecture, or Sparc, concept, is putting the chip set through its paces in a new work station under development.

The E100 Clipper from Intergraph's Advanced Processor Division in Palo Alto, Calif., meanwhile, will make use of high-speed ECL gate arrays as well as a dozen application-specific integrated circuits, according to the division's director of sales and marketing, Ralph Kaplan. Performance target is 70 mips and 12 double-precision Linpack megaflops, which puts it four to five times faster than Intergraph's 50-MHz, 14-mips CMOS C300 Clipper module.

The three circuit boards holding the E100 will reside in a liquid-cooled "fish tank," Kaplan says. This will form the core of a compute server for a network of Intergraph work stations. The server will not be cheap: about $250,000 for a minimum configuration with 64 Mbytes of main memory.

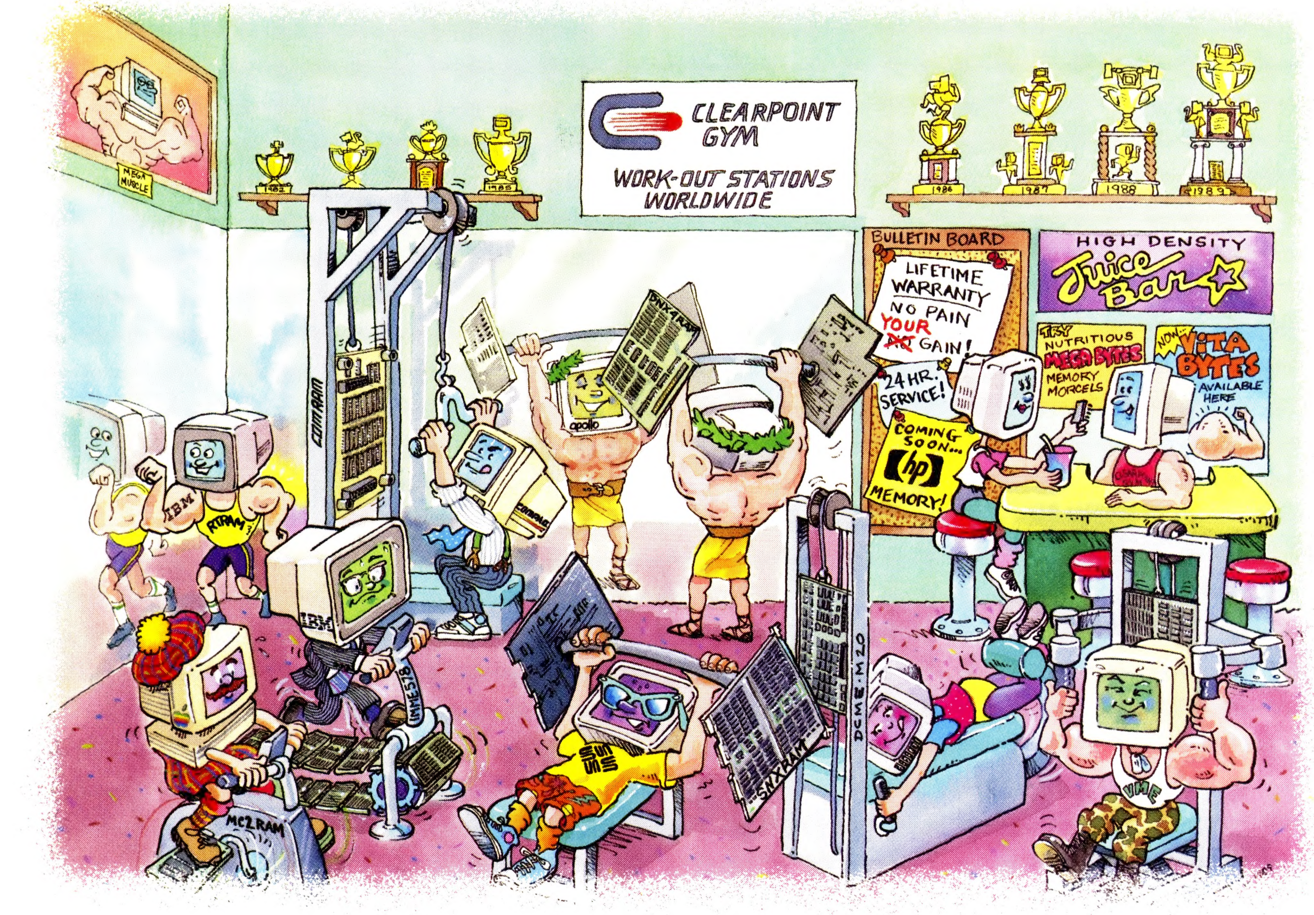
The company will offer samples of a 16-mips, 60-MHz module by year's end to go along with sets performing 10 mips at 40 MHz and 14 mips at 50 MHz. (Intergraph just began offering a die shrink of its original C100 for less than $200 in volume quantities. It will do 6 mips at 25 MHz or 8 mips at 33 MHz.)

The company also recently unveiled plans for offering in 1990 a wider 128-bit Clipper bus, as well as the present 32-bit width. This could lead to 47-mips operation with a 70-MHz clock sometime in 1993.

Performance jumps in CMOS also came from Cypress Semiconductor Corp. of San Jose, Calif. Last summer Cypress announced 29-mips, 40-MHz Sparc chips based on the same design as its 24-mips CY7C601 integer unit unveiled earlier this year. Such performance gains point the way to the future, says Steve Goldstein, director of marketing of Ross Technology Inc., the Sparc-development arm of Cypress. From the first CMOS microprocessor, Motorola's 68020, which in 1984 had a 12-MHz clock speed, the industry "has moved to 40 MHz in 1989, having gained a multiple of 3.3," Goldstein points out.

He sees no reason why the industry could not achieve a similar jump in processor speed in the next half decade, "maybe to 100 or 120 MHz over the next five years. This could be done with CMOS technology coupled, perhaps, to bipolar enhancements for the critical paths [biCMOS]," Goldstein says. *–Alfred Rosenblatt*

Pump Up Your Performance



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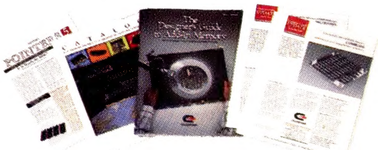

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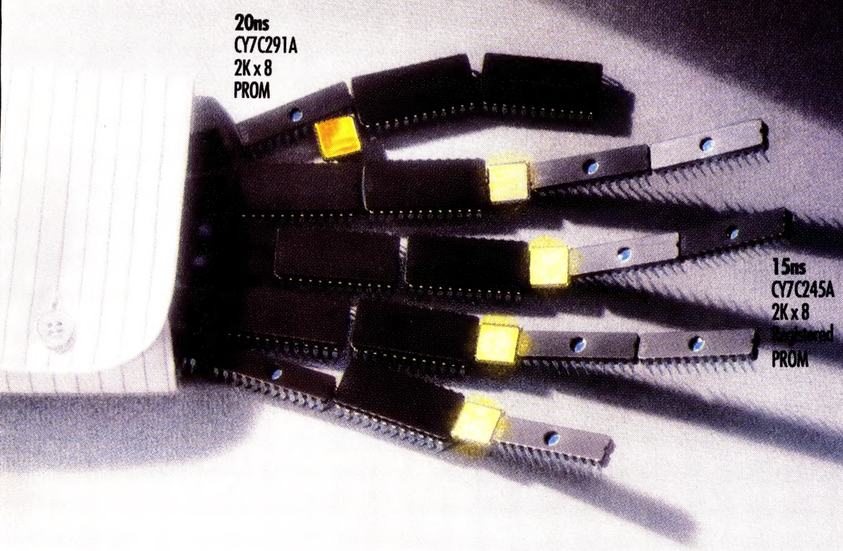

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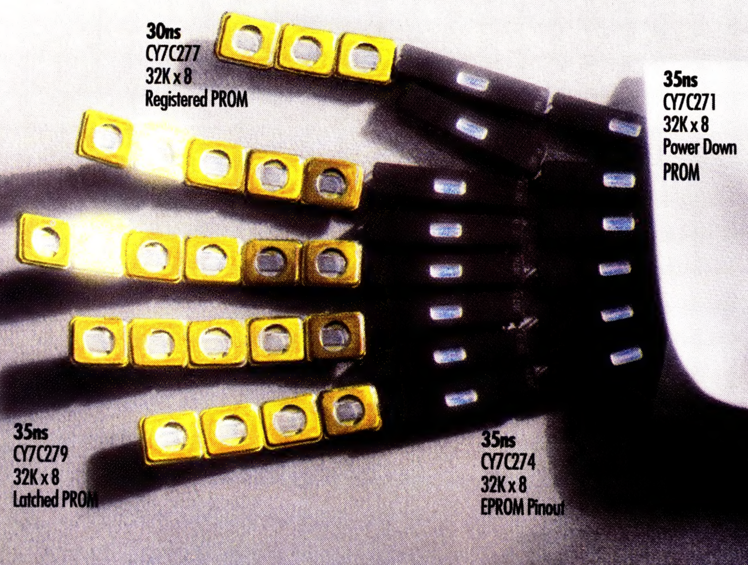

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